Adaptive Scheduling for Systems with Asymmetric Memory Hierarchies

Po-An Tsai, Changping Chen, and Daniel Sanchez

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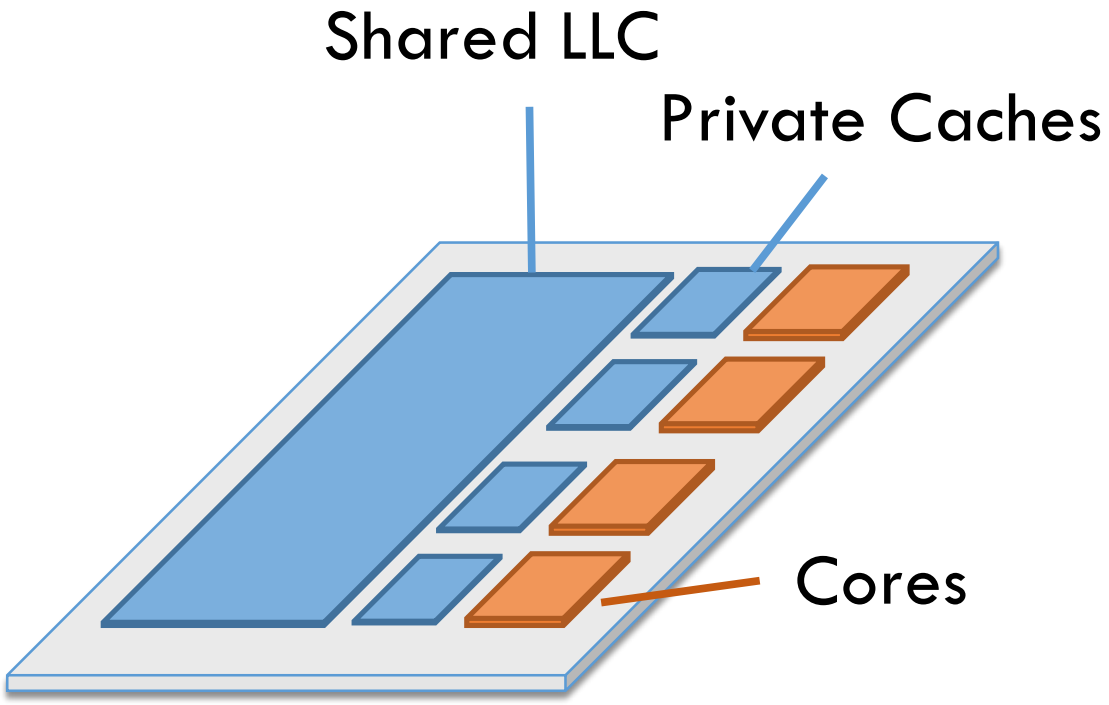

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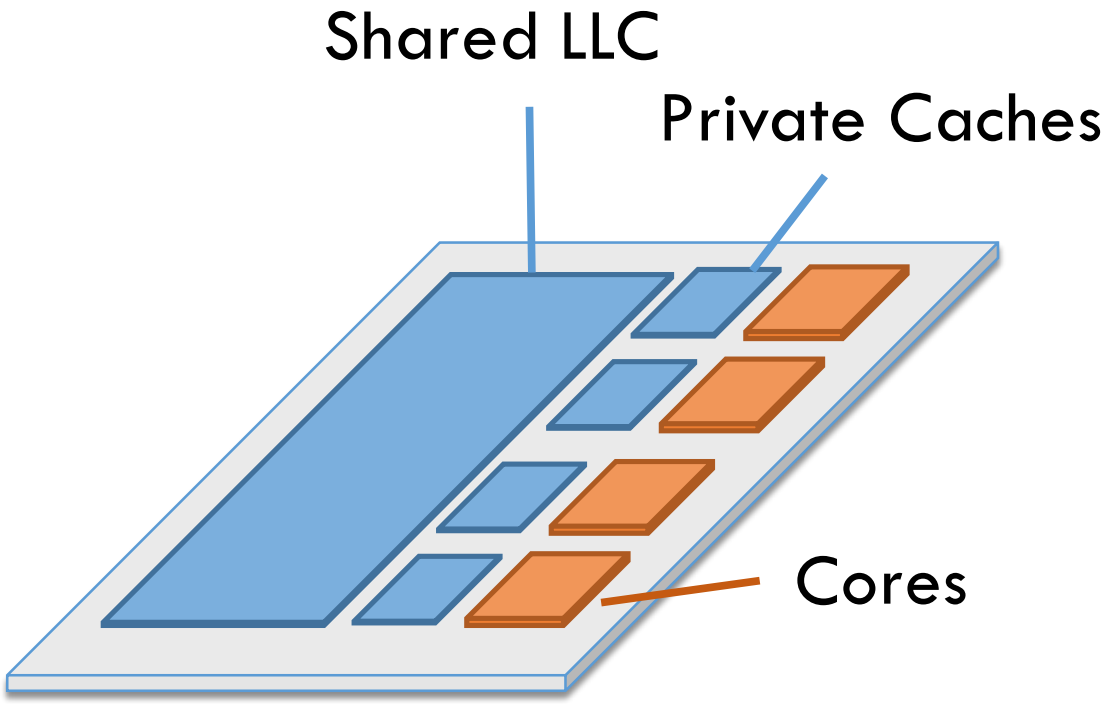

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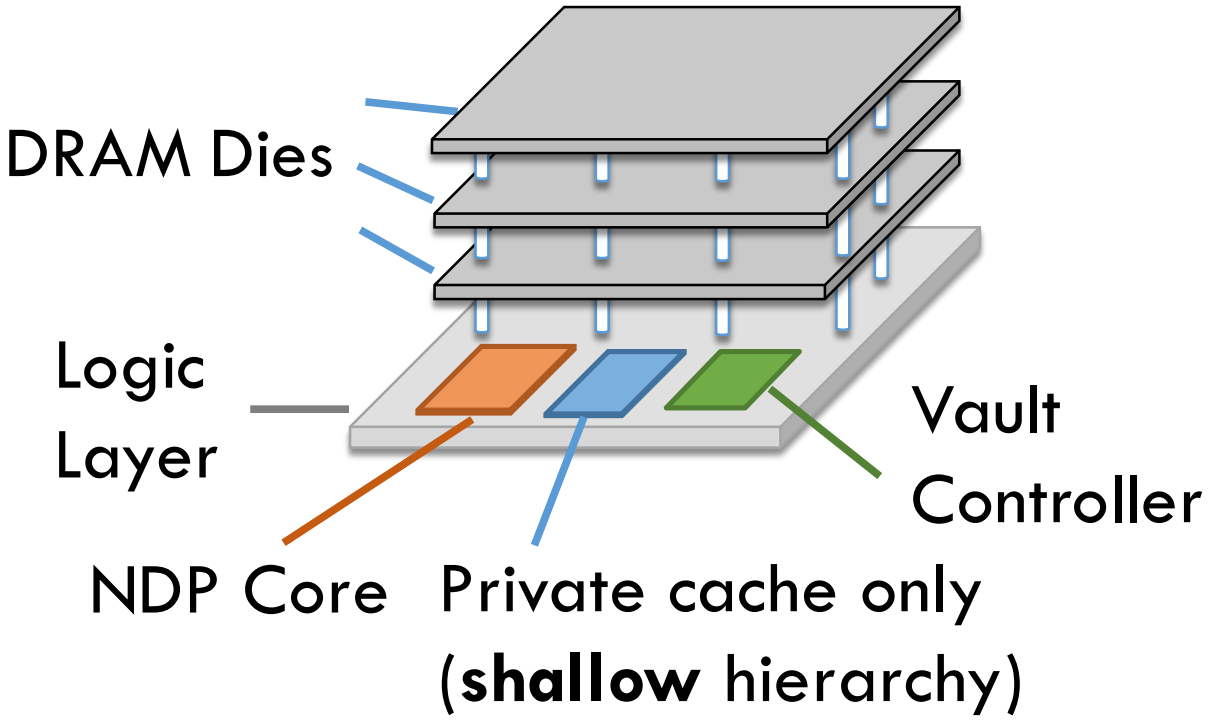

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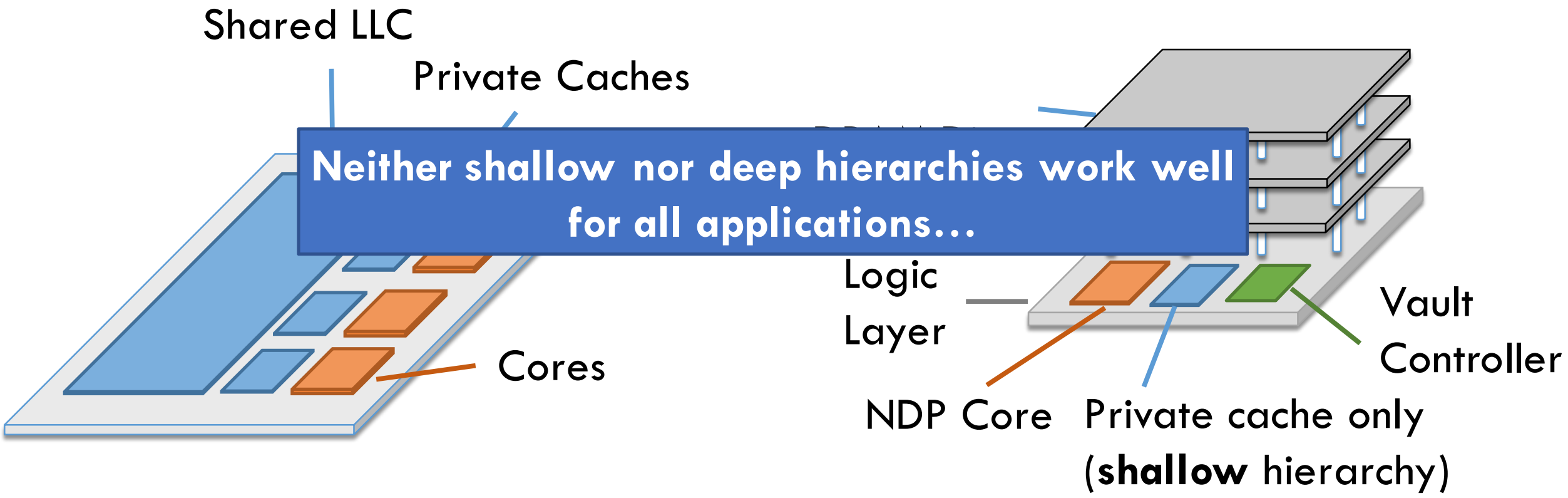

Neither shallow nor deep hierarchies work well for all applications…

Asymmetric hierarchies get the best of both worlds

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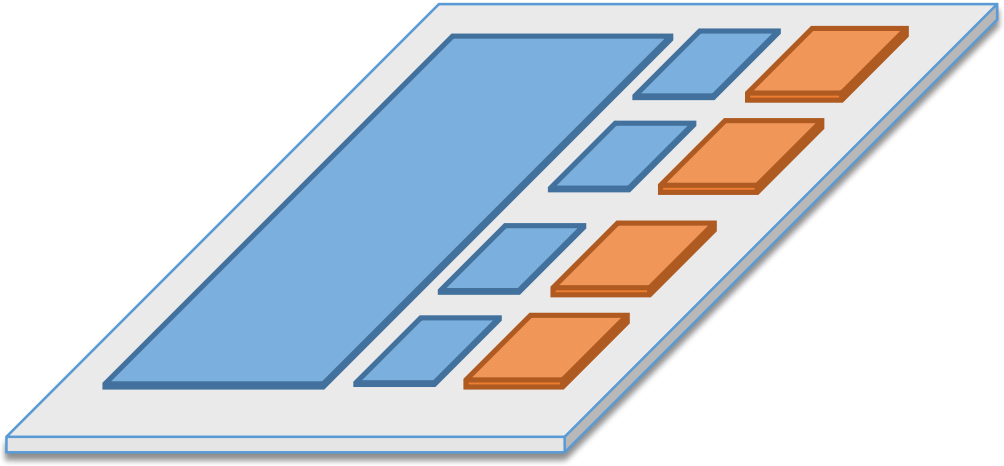
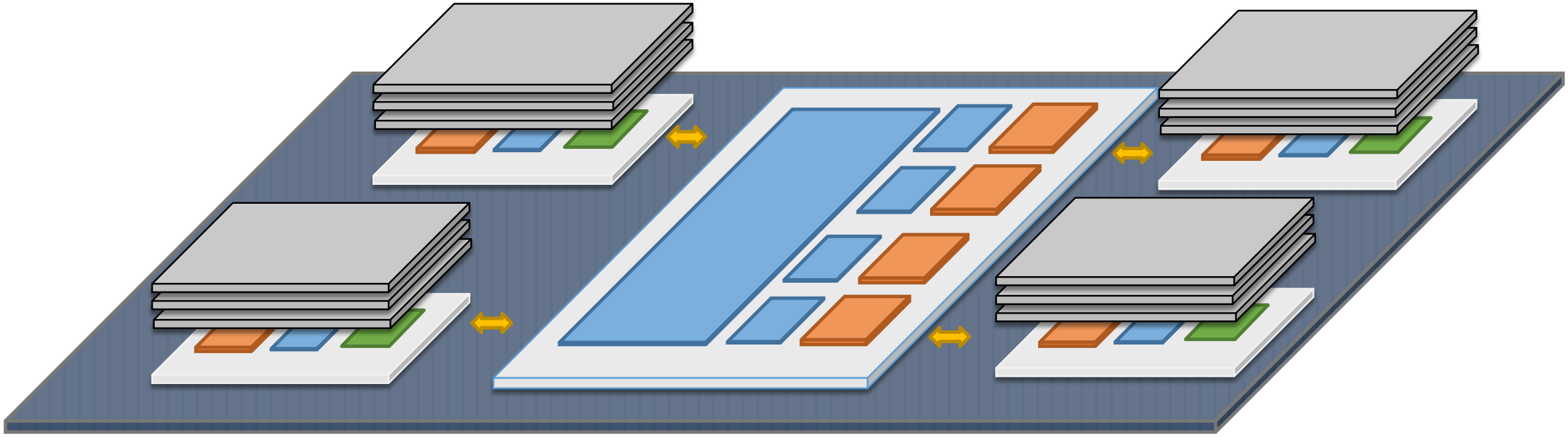


Asymmetric hierarchies get the best of both worlds

Prior work proposes hybrid system with asymmetric memory hierarchies to get the best of both



[Ahn et al., ISCA'15][Gao et al., PACT'15]
[Hsieh et al., ISCA'16][Boroumand et al., ASPLOS'18]

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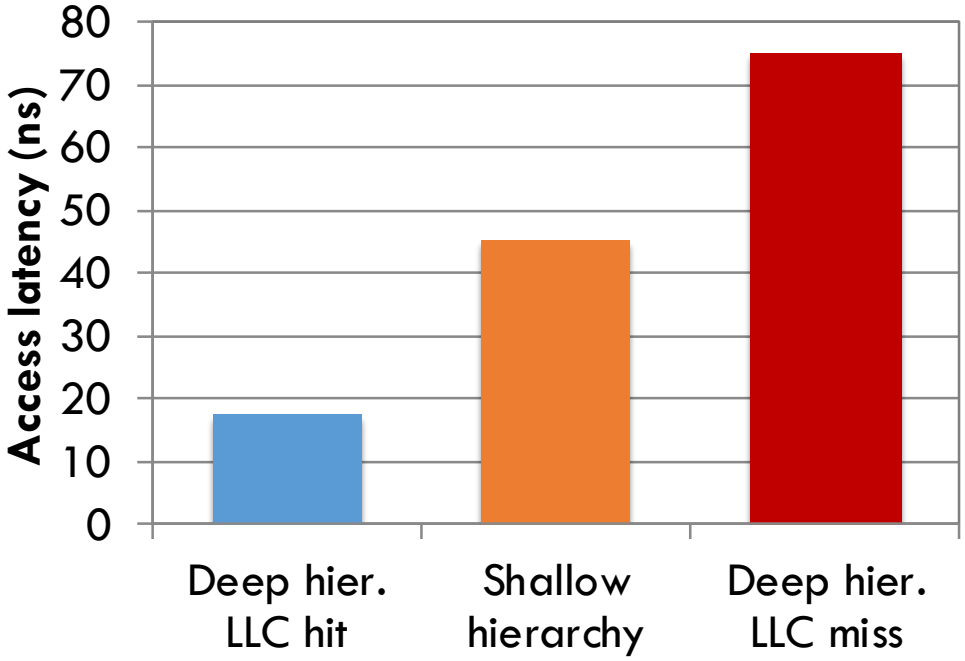

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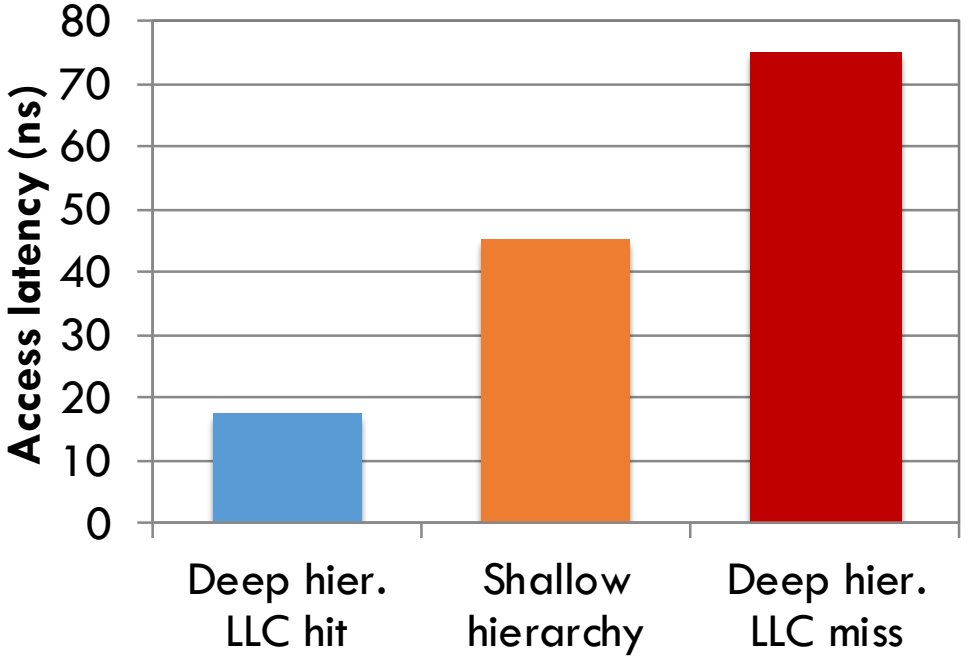

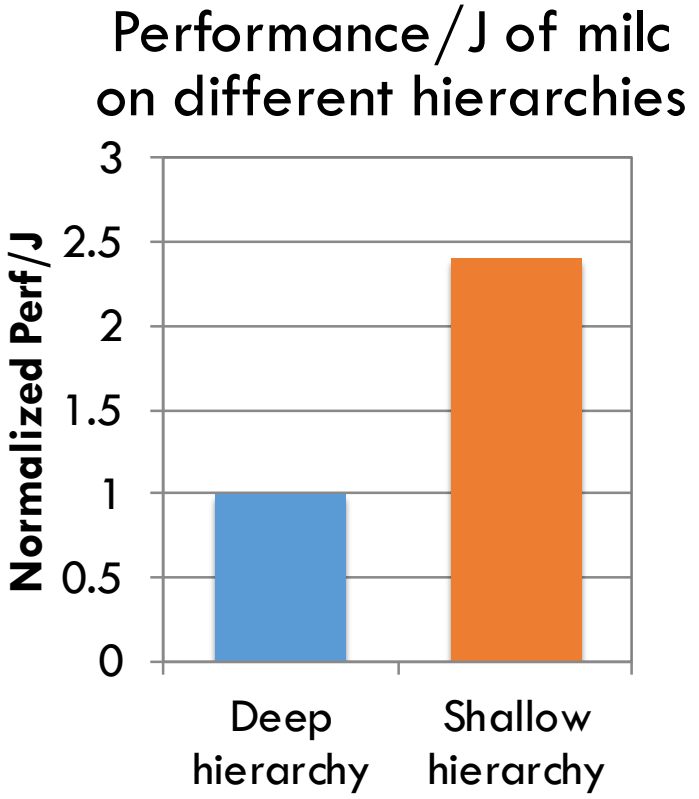

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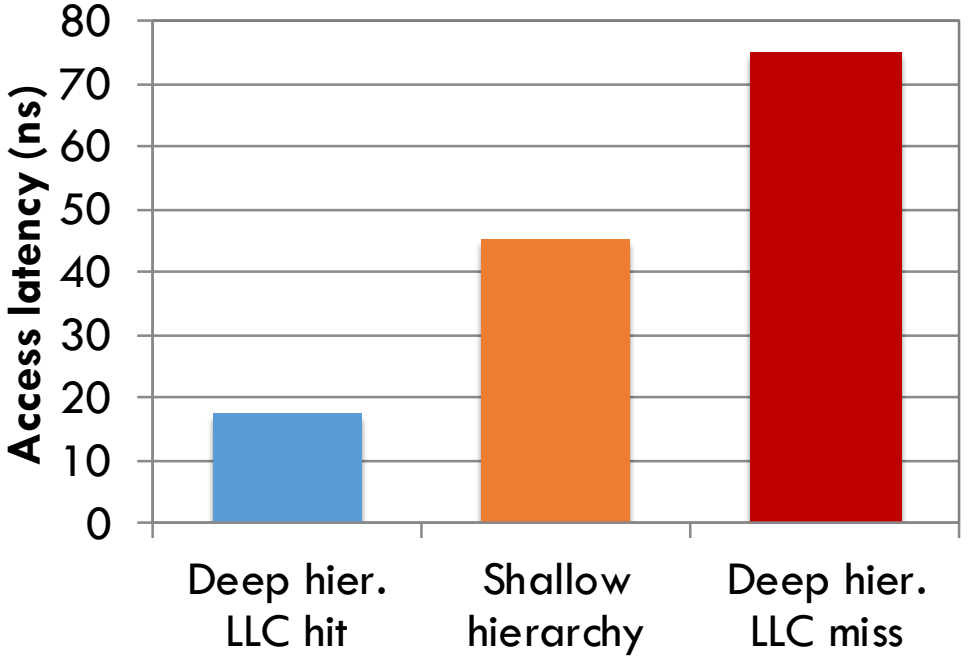

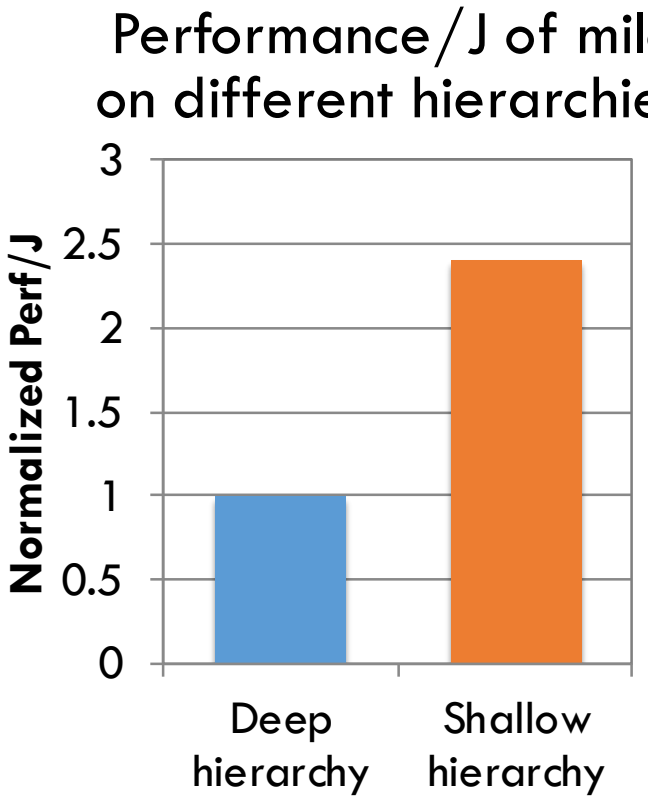

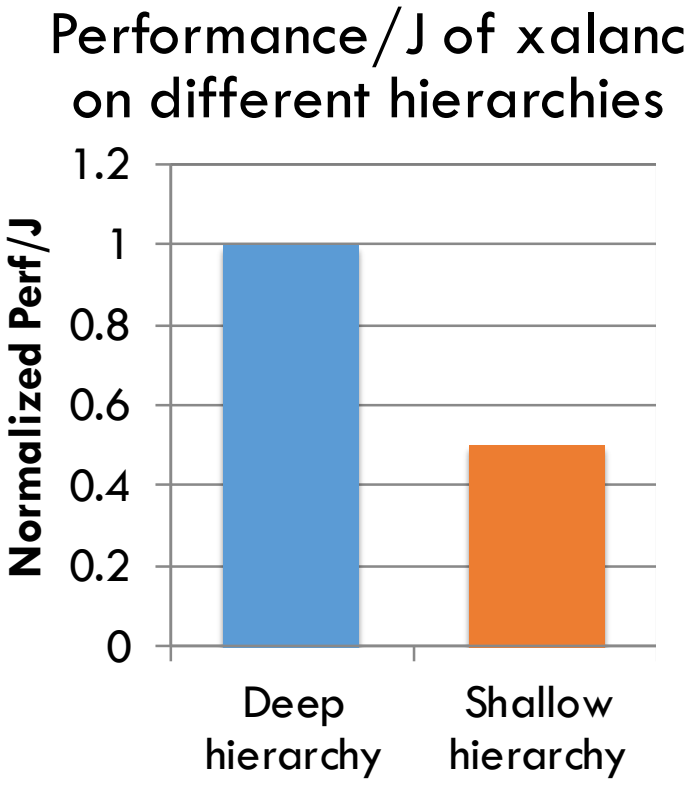

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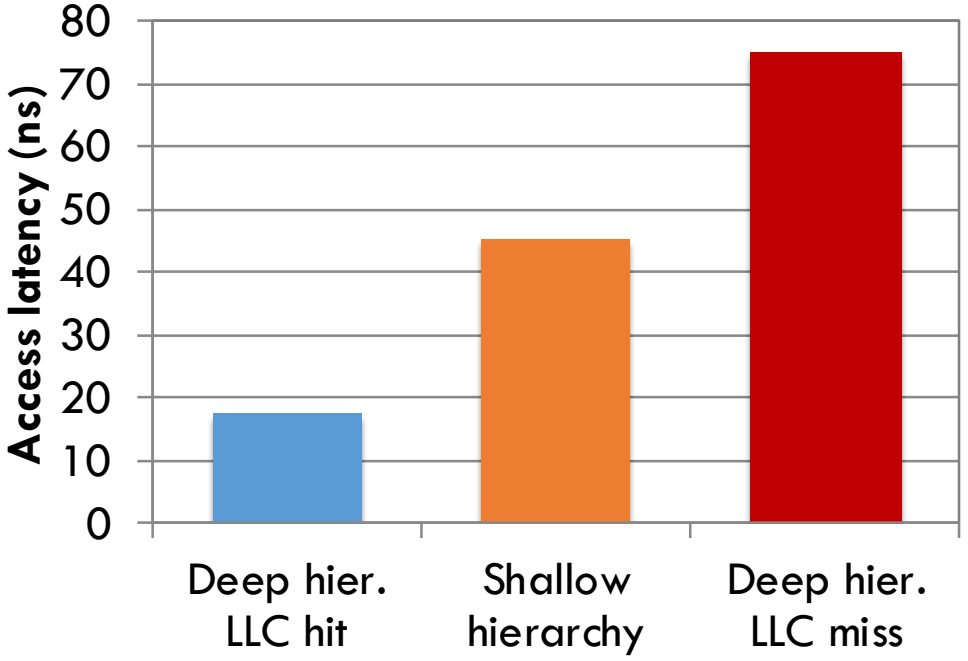

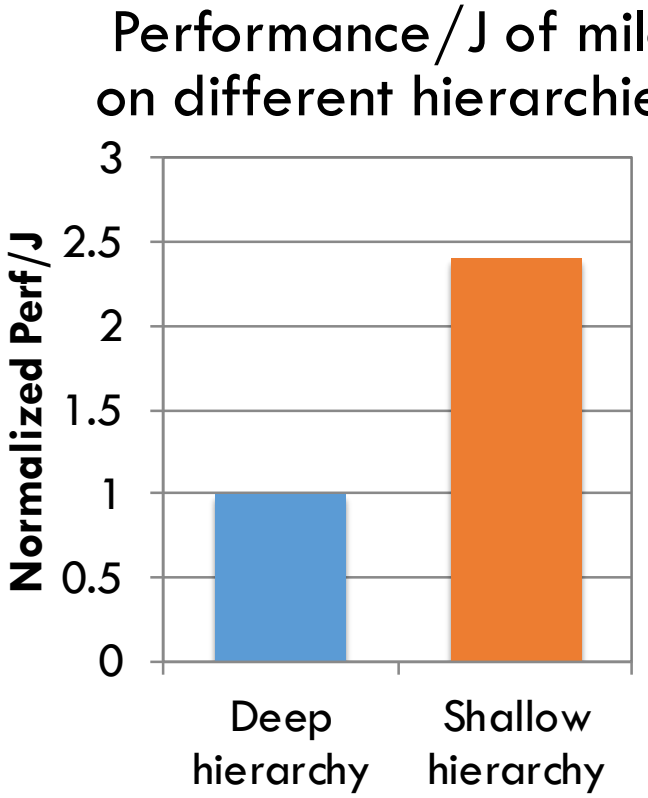

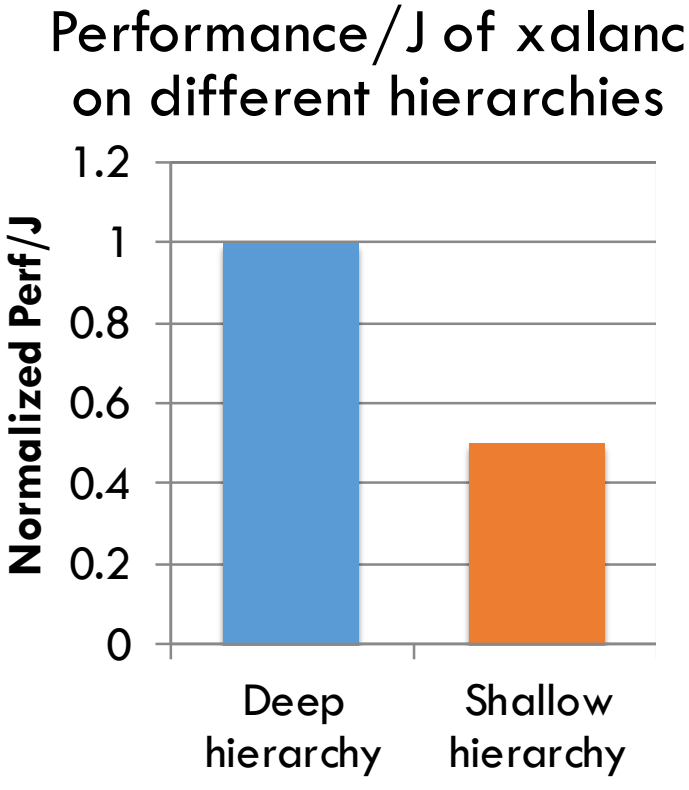

How well each application can use the shared LLC is critical to its preference

Scheduling programs to the right hierarchy is hard

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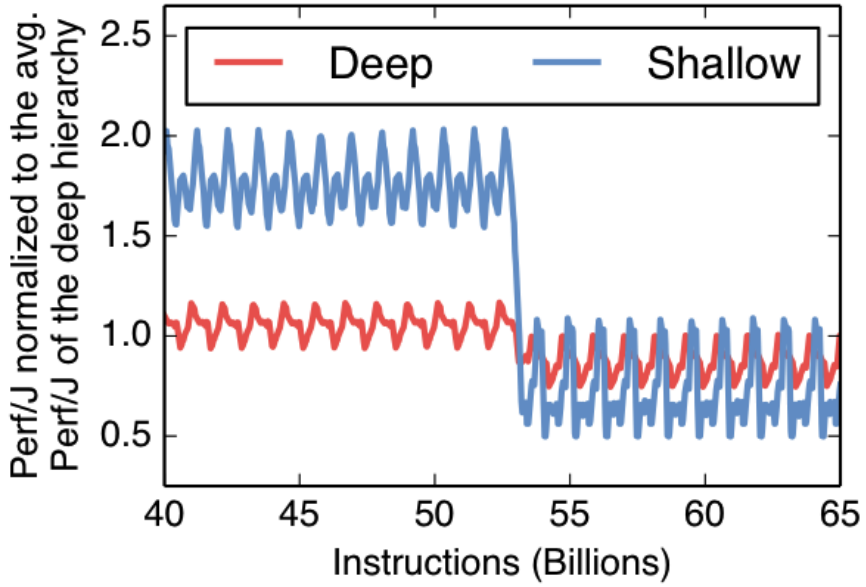

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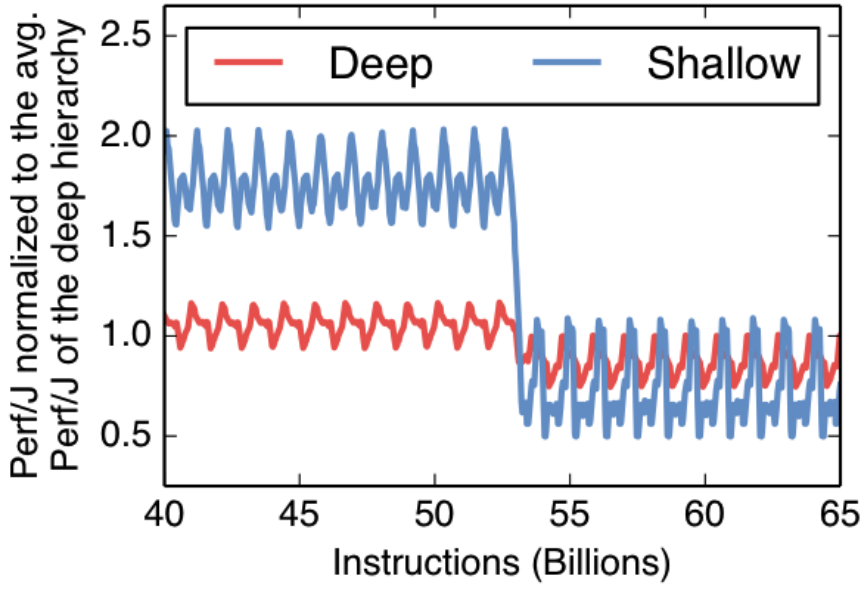

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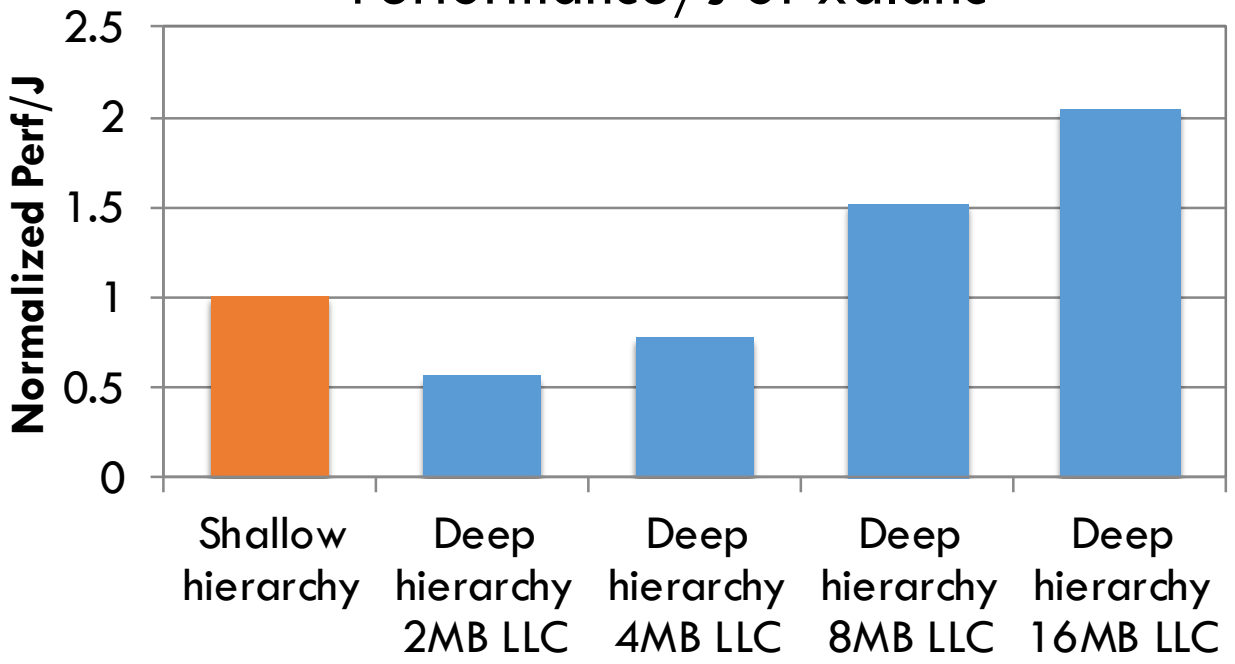

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Applications may prefer different hierarchies due to resource contention with other applications

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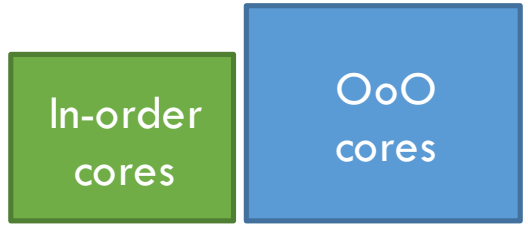

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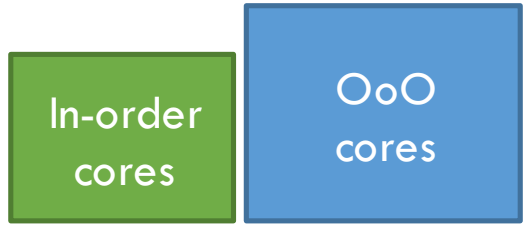

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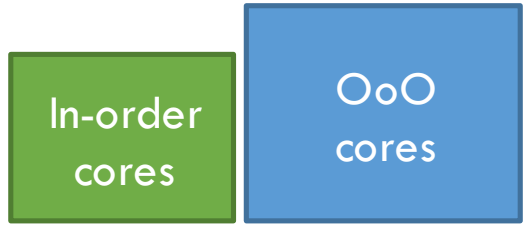

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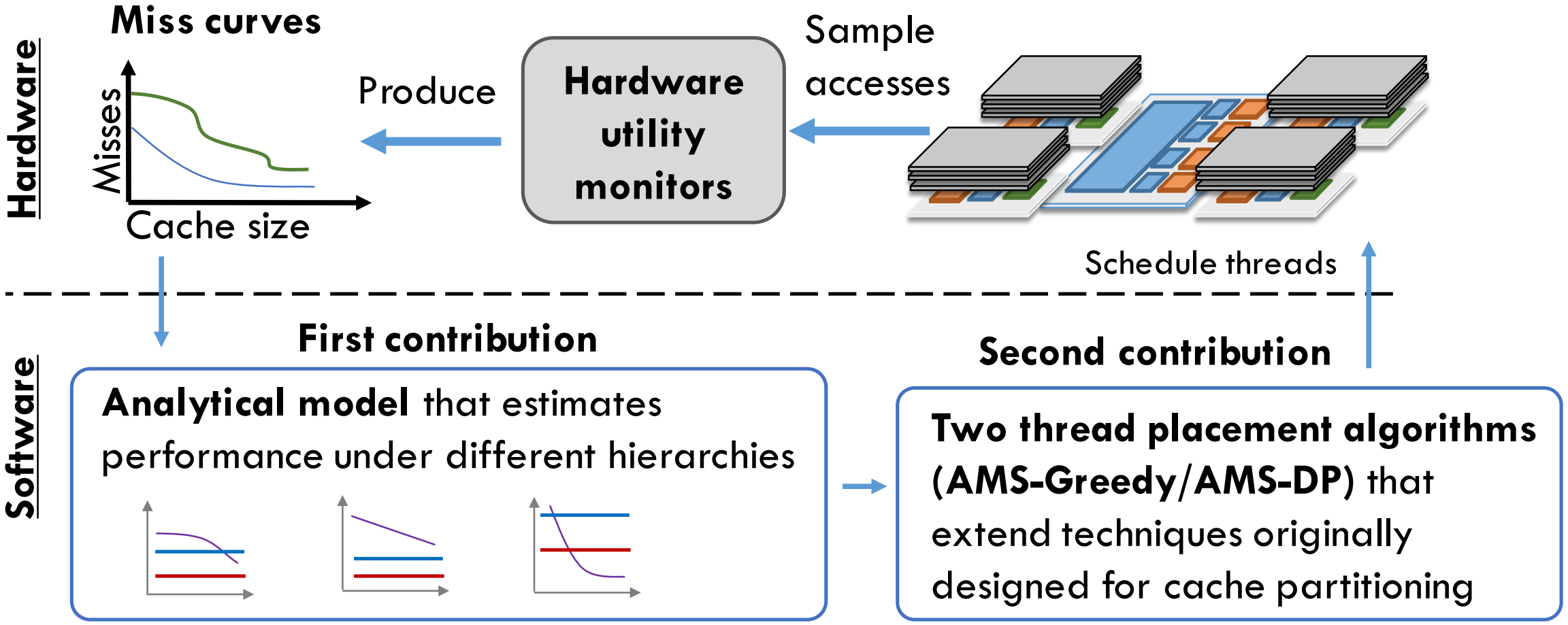
By contrast, our goal is to schedule threads considering both memory and core asymmetries, with no program modifications and transparently to users

AMS: An asymmetry-aware scheduler



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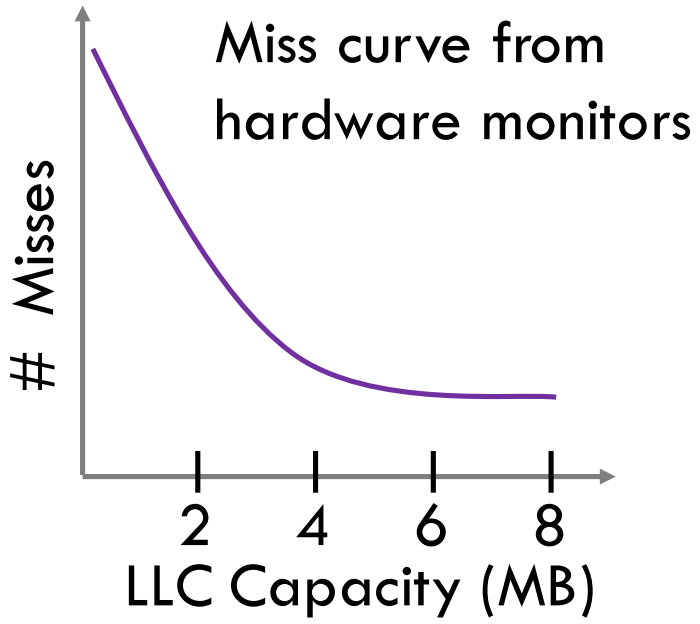

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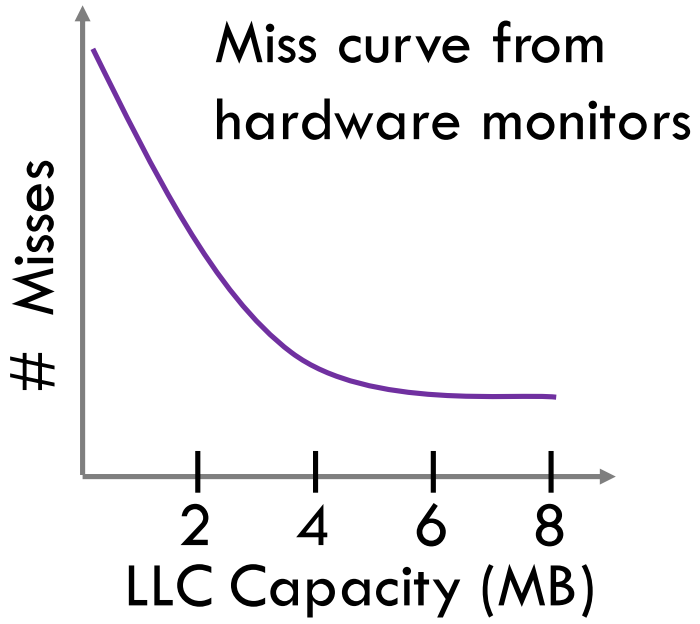

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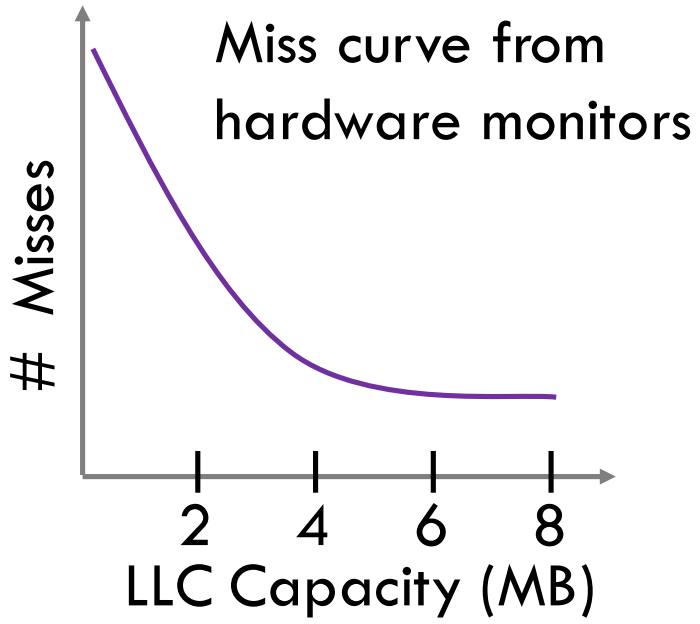

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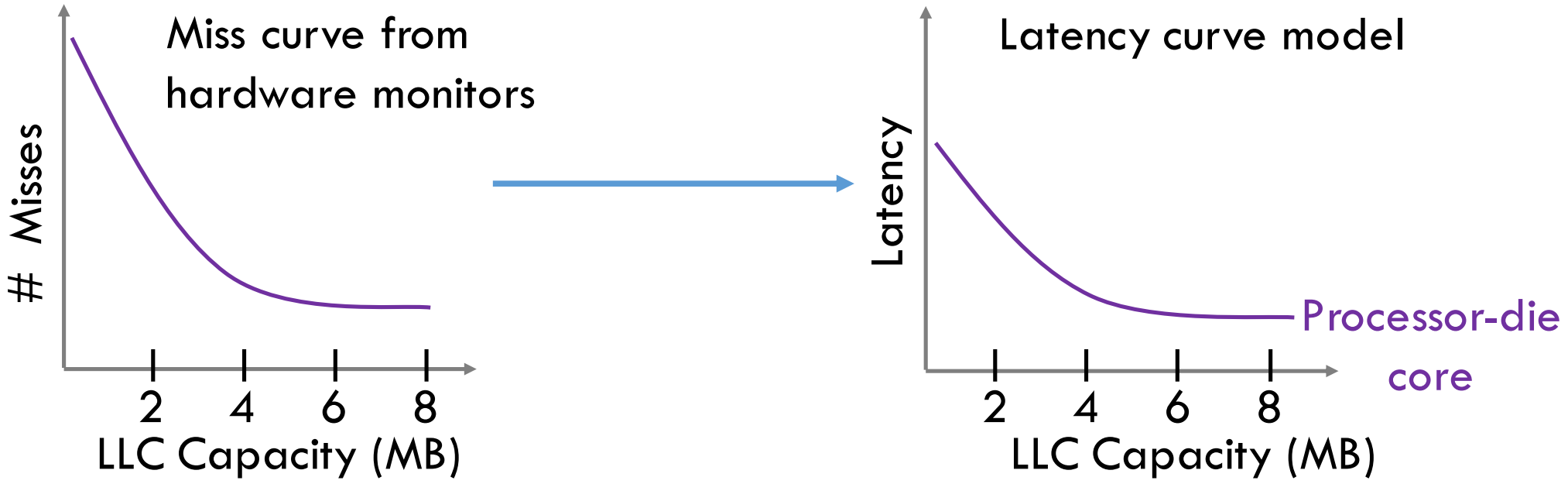

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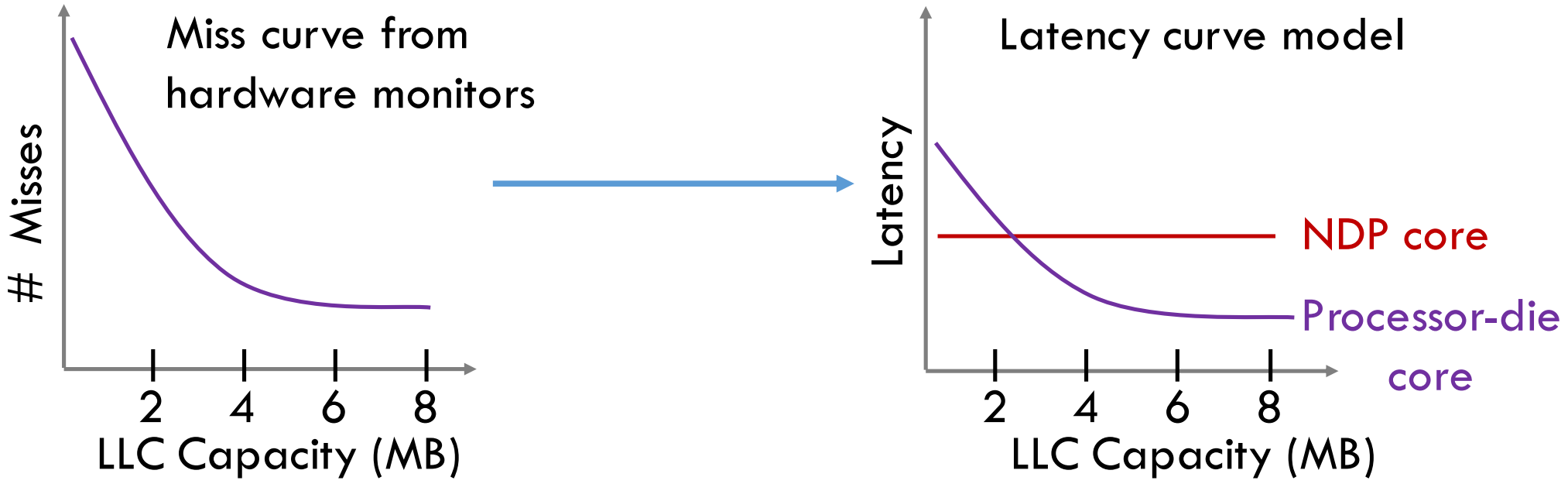

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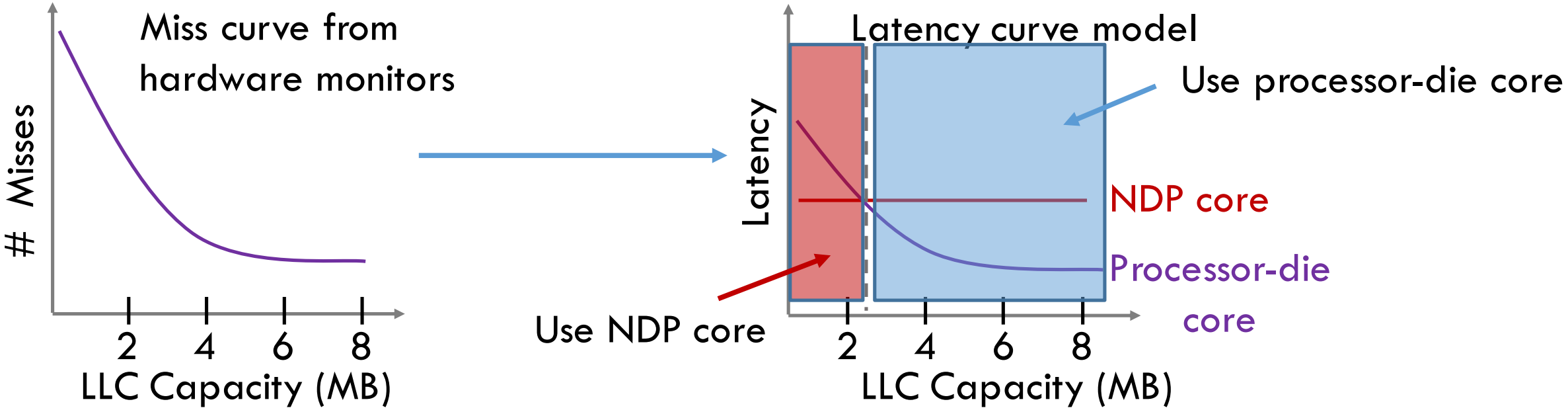

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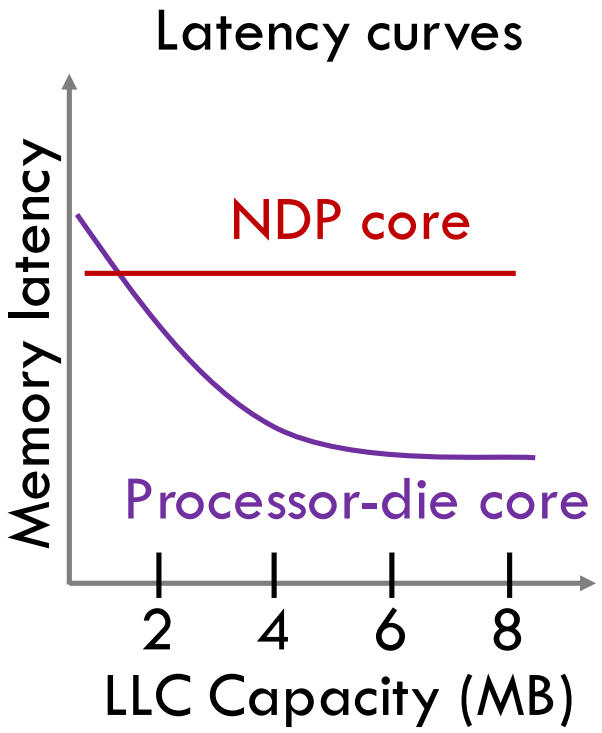

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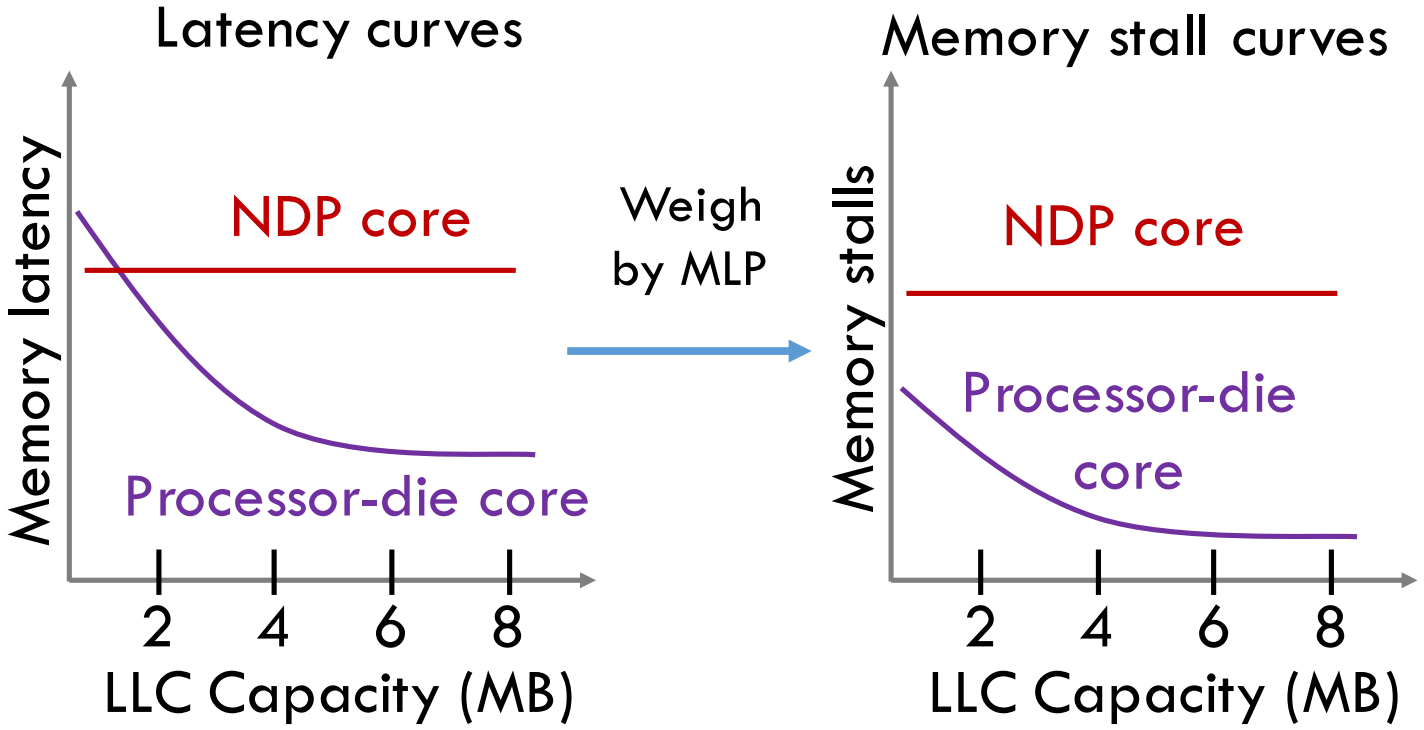

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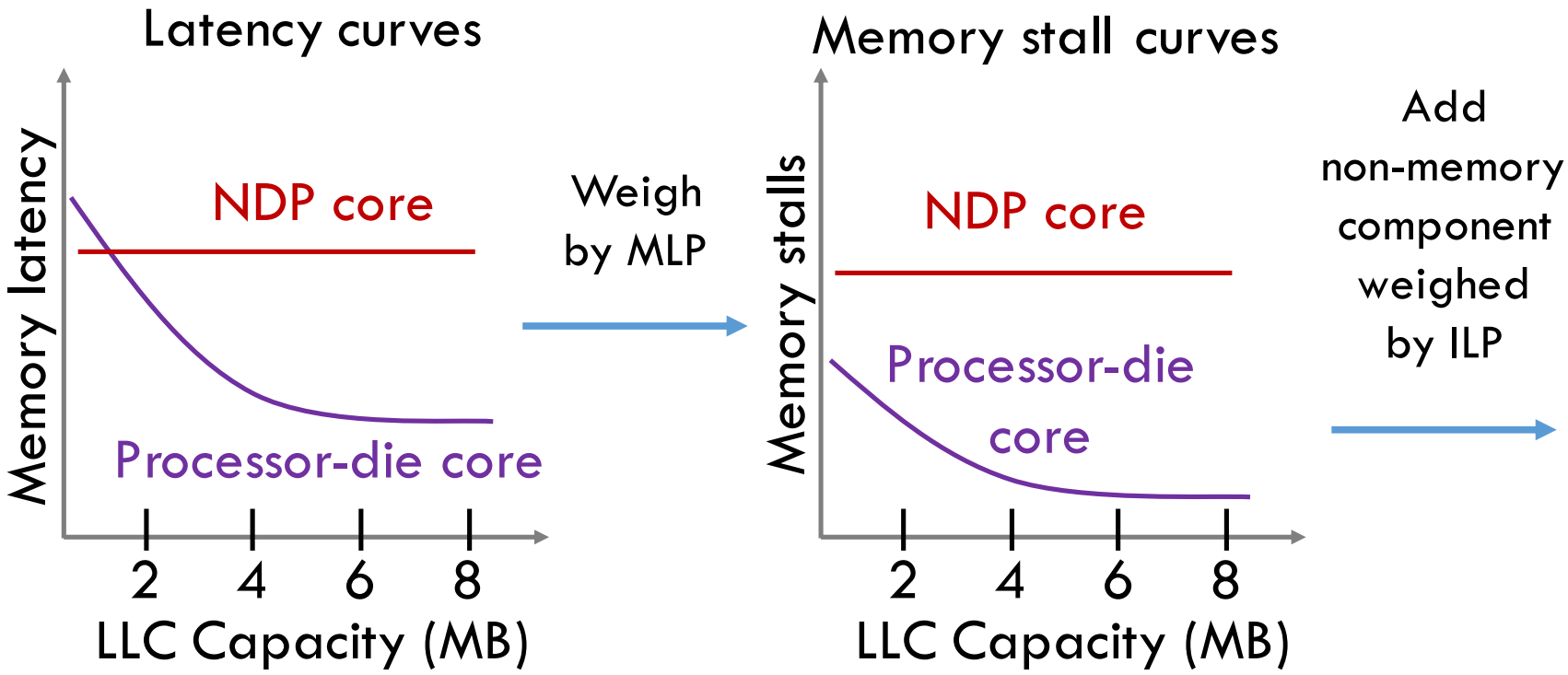

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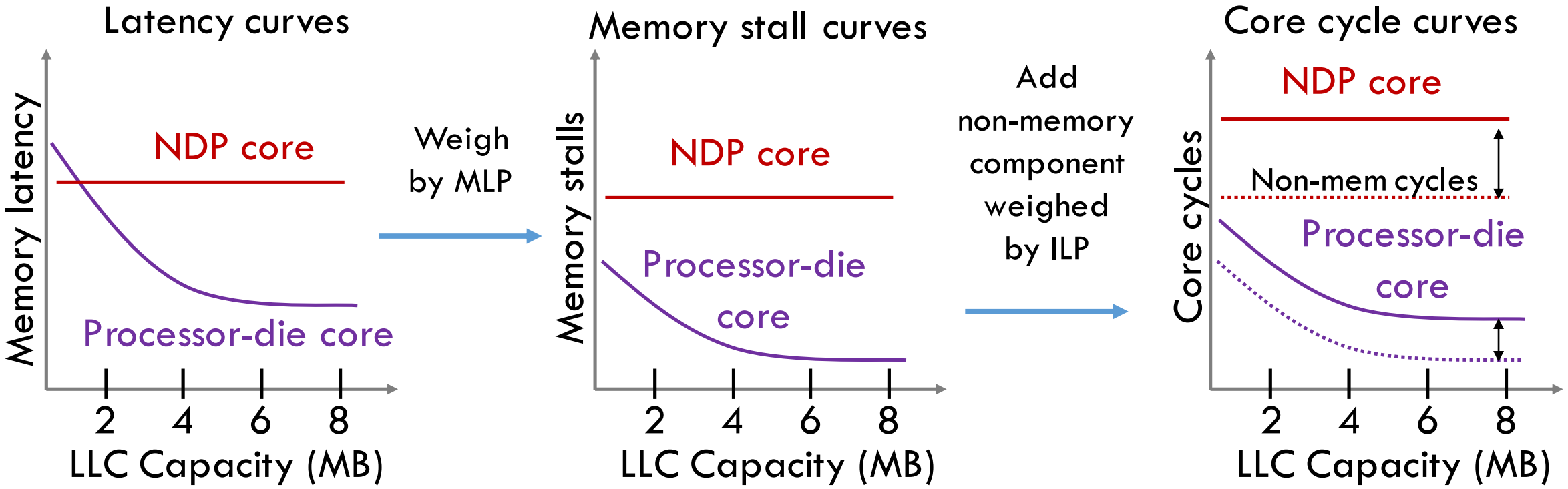

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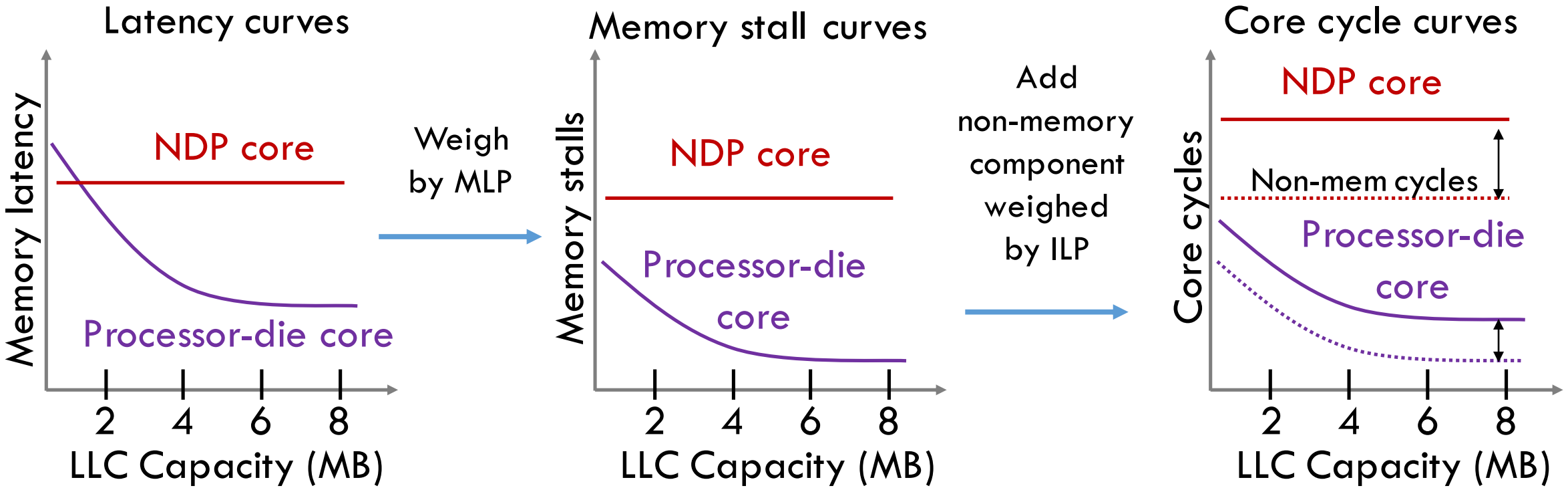

Can be extended to other asymmetries, like frequencies (see paper)

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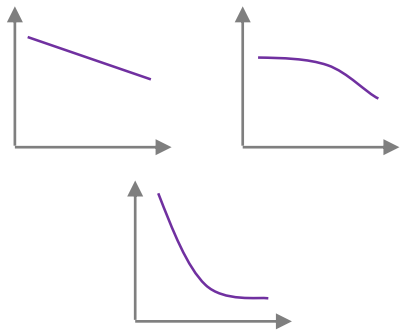
Input:
Cost curves of all threads for deep hierarchy



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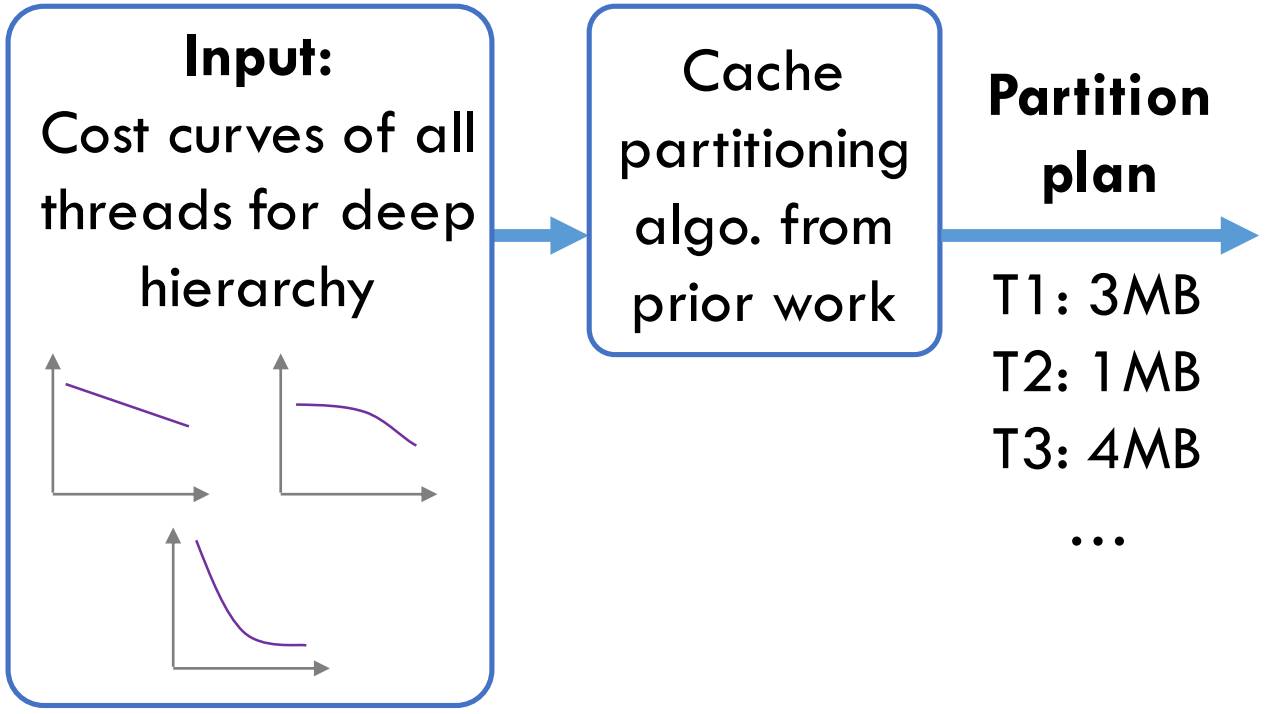

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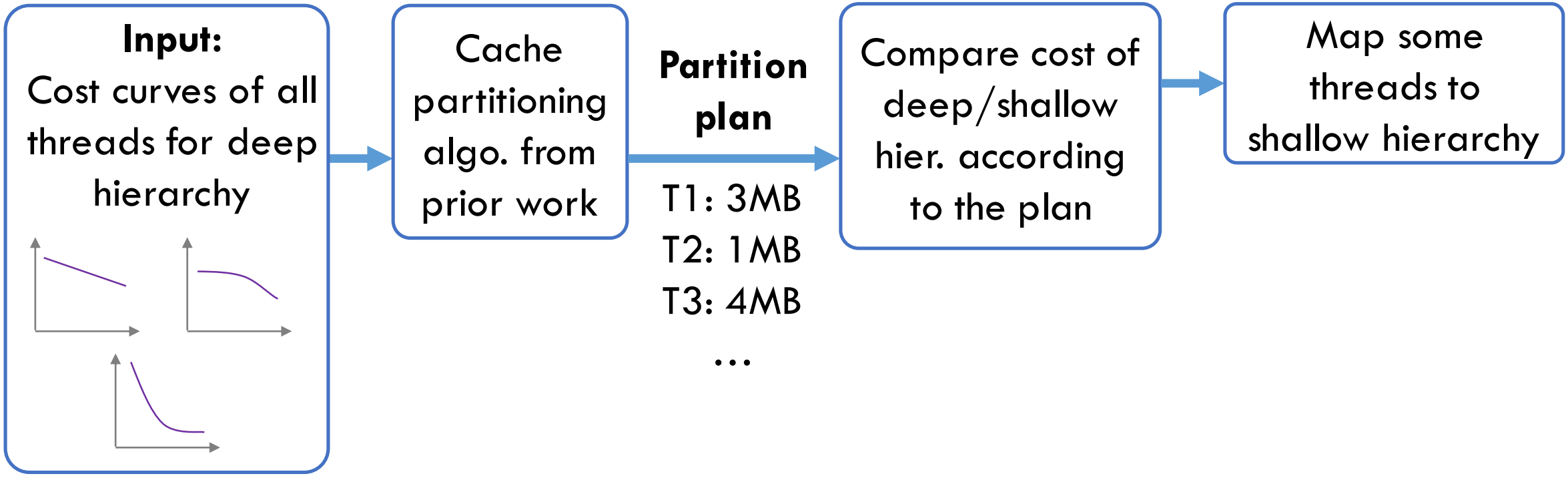

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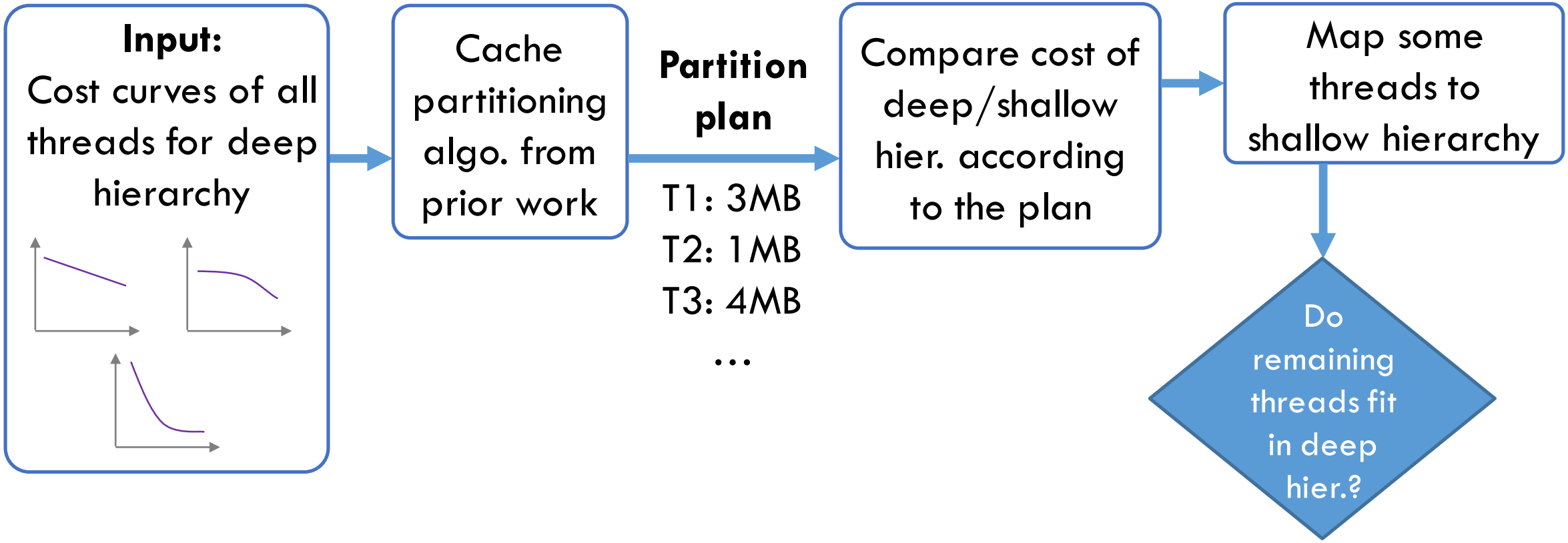

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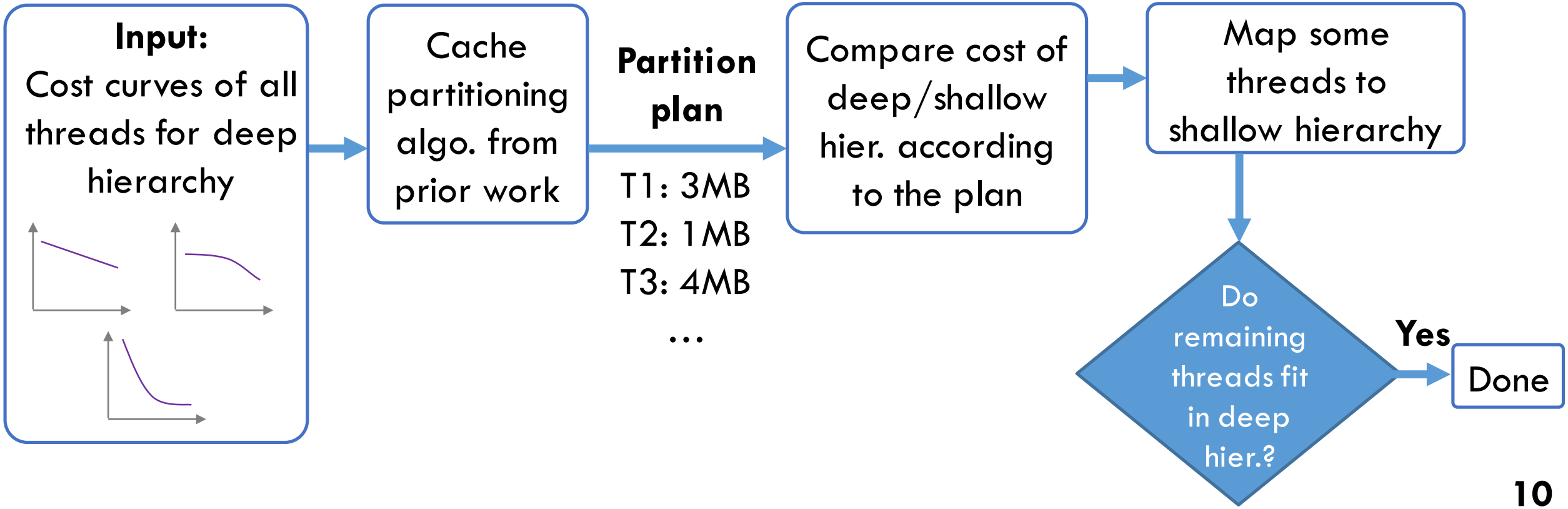

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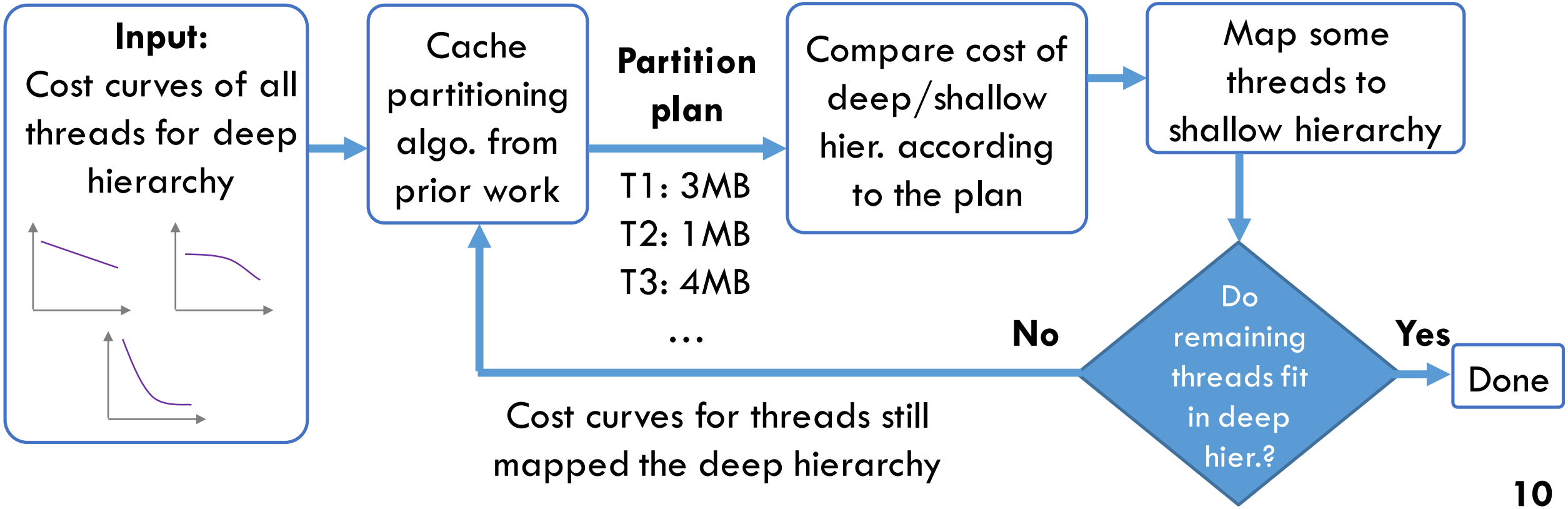

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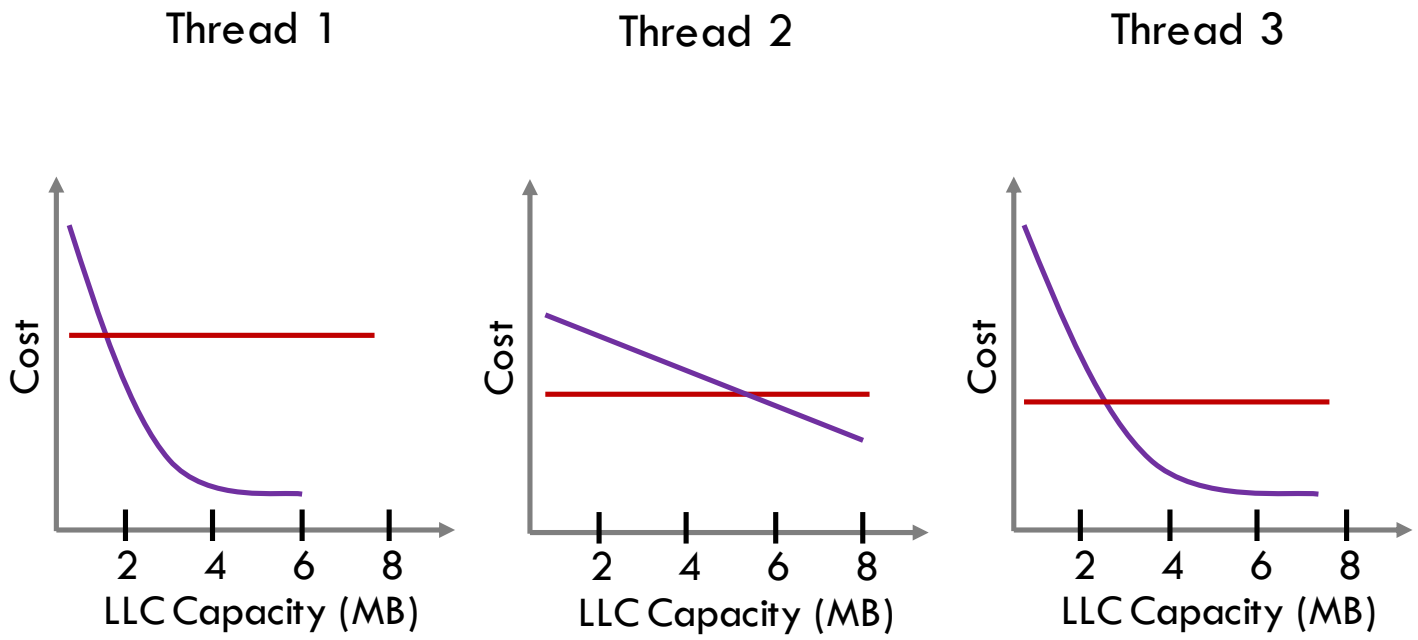

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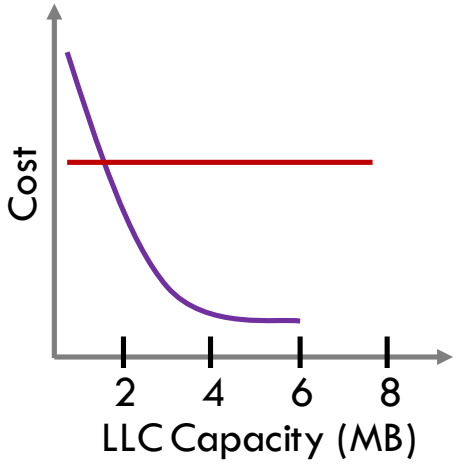
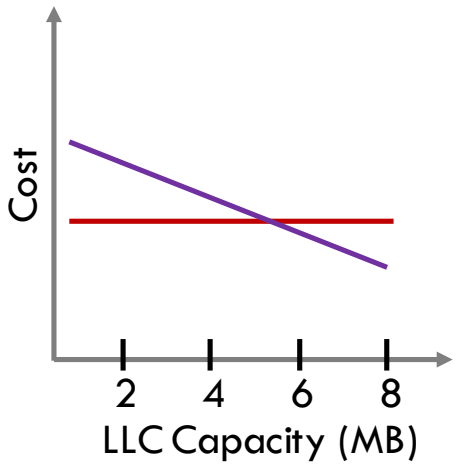
Partition the LLC among threads 1-3

8MB

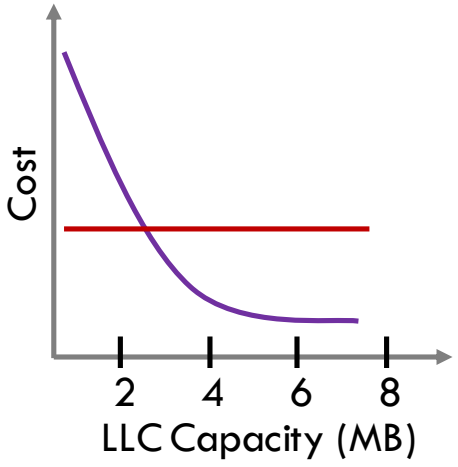
Thread 1



Thread 2



Thread 3



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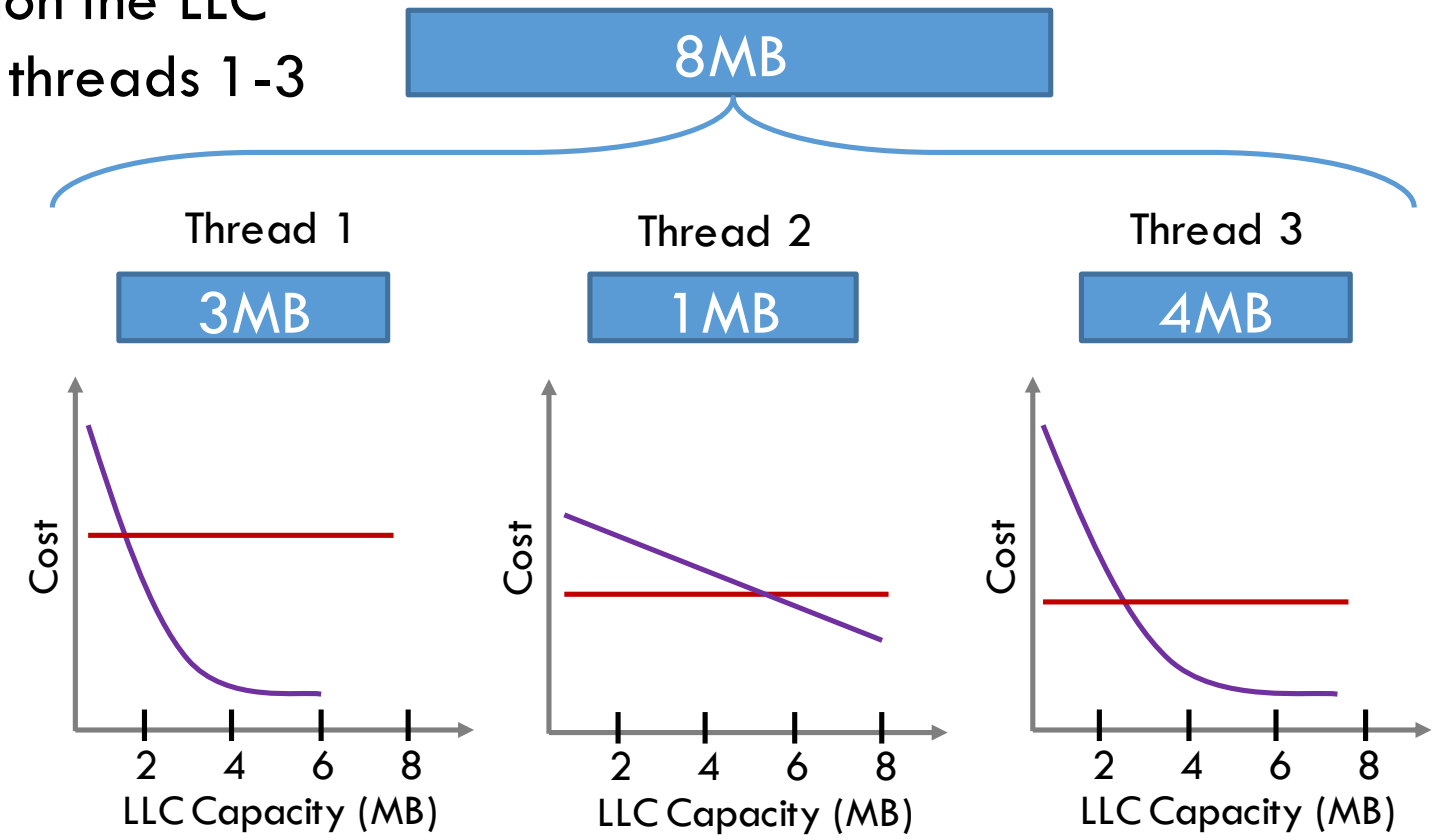

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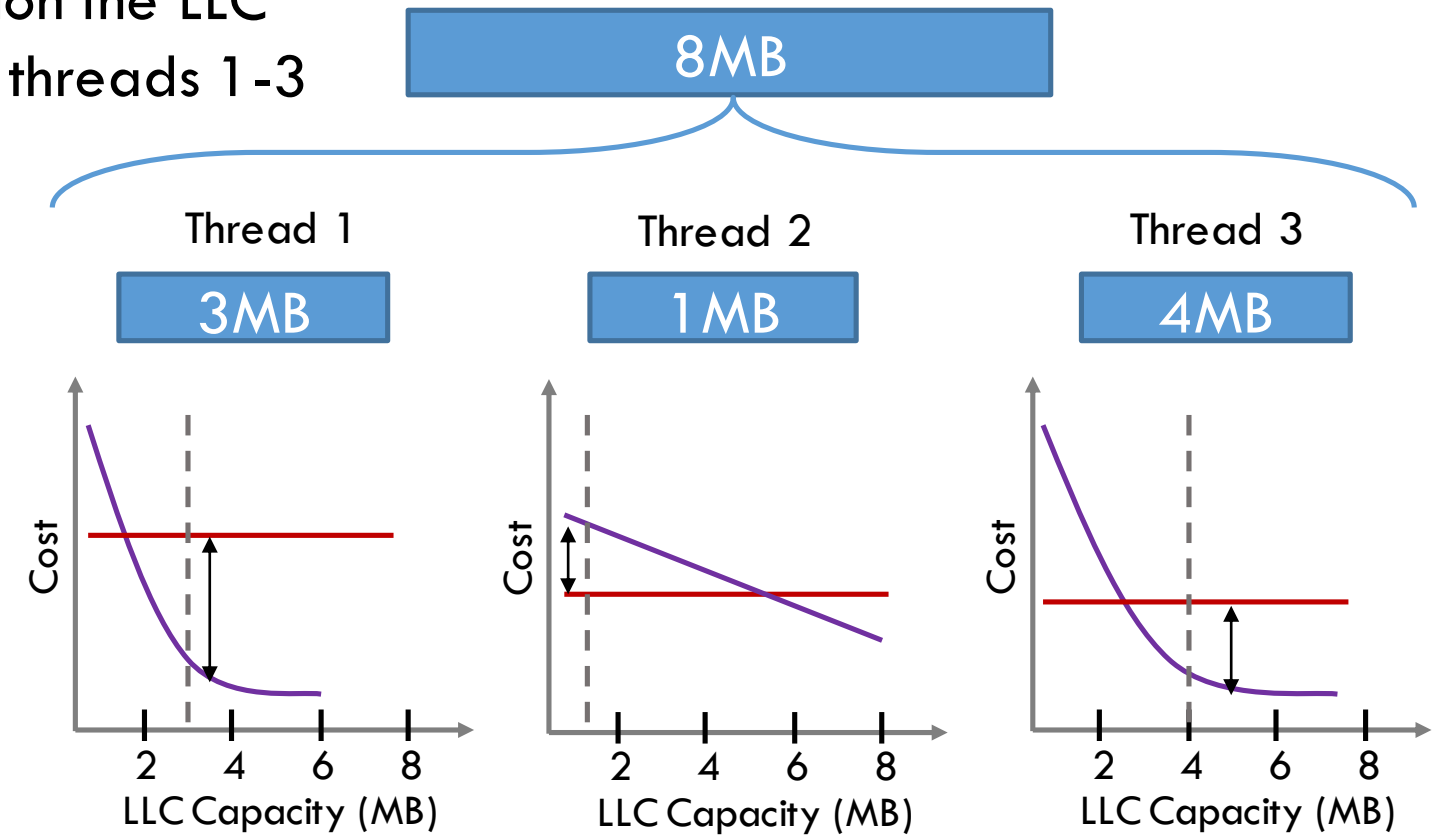

⟷ : **Opportunity cost**

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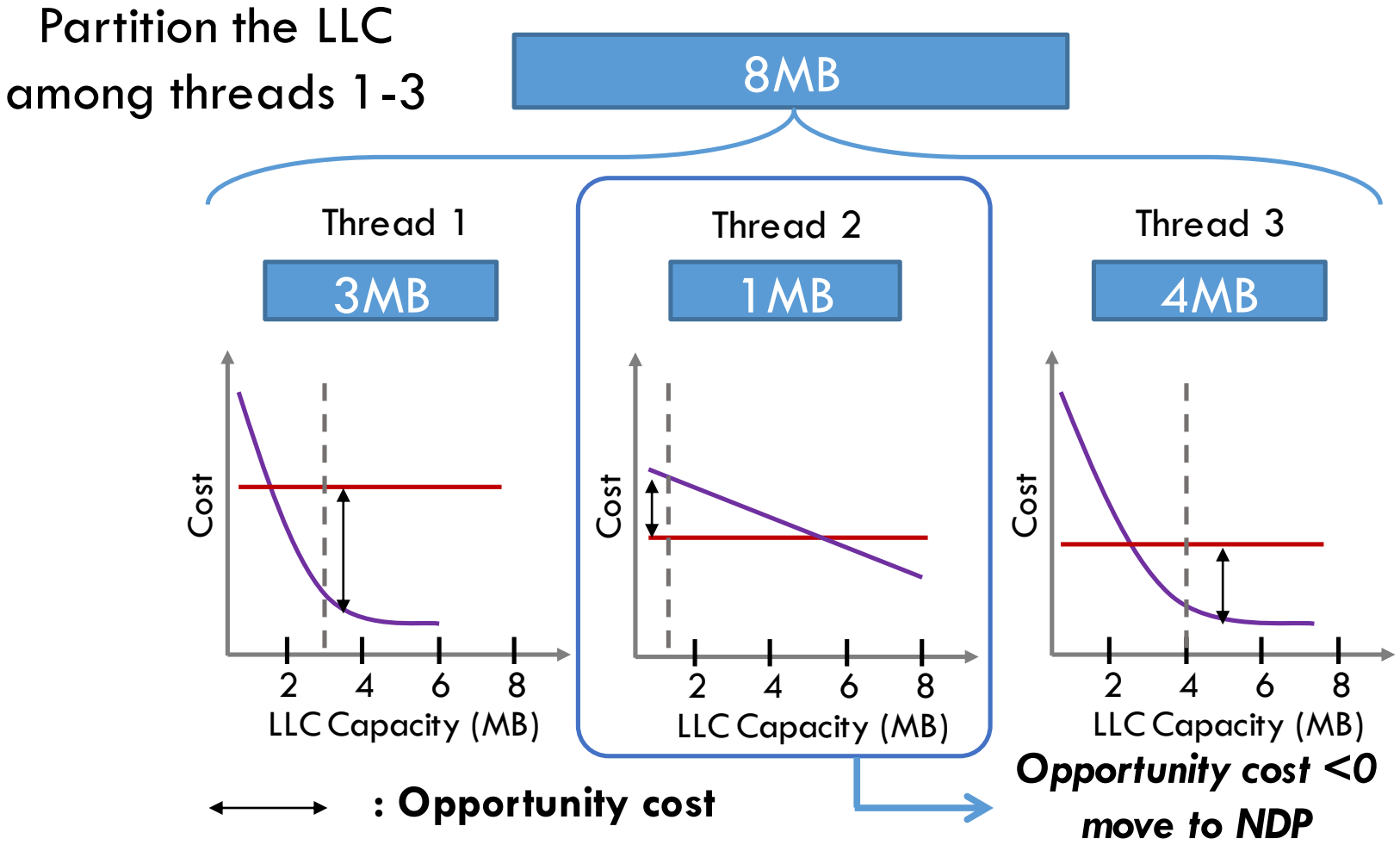

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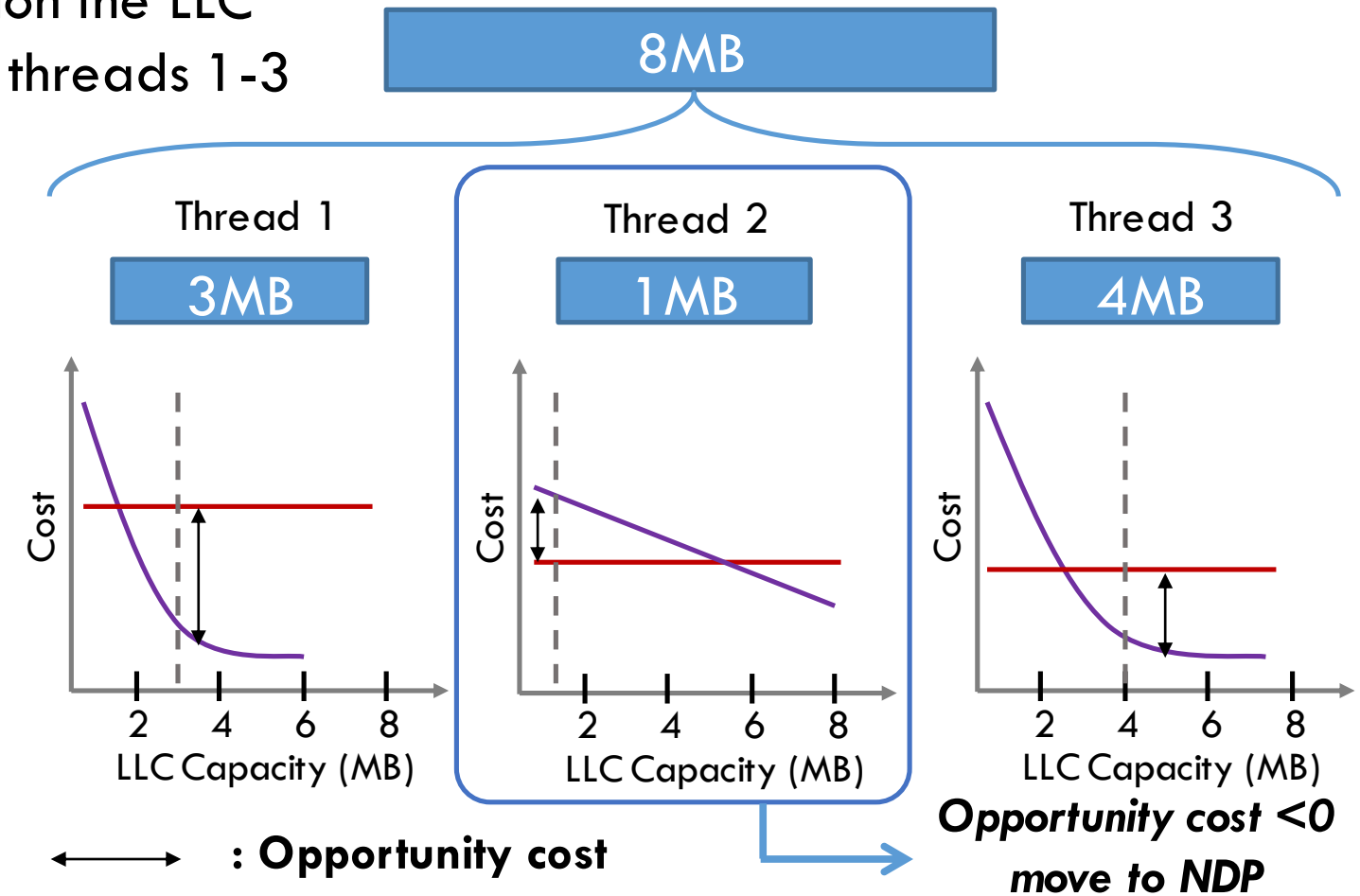

Perform multiple rounds of partitioning until the processor die is not oversubscribed

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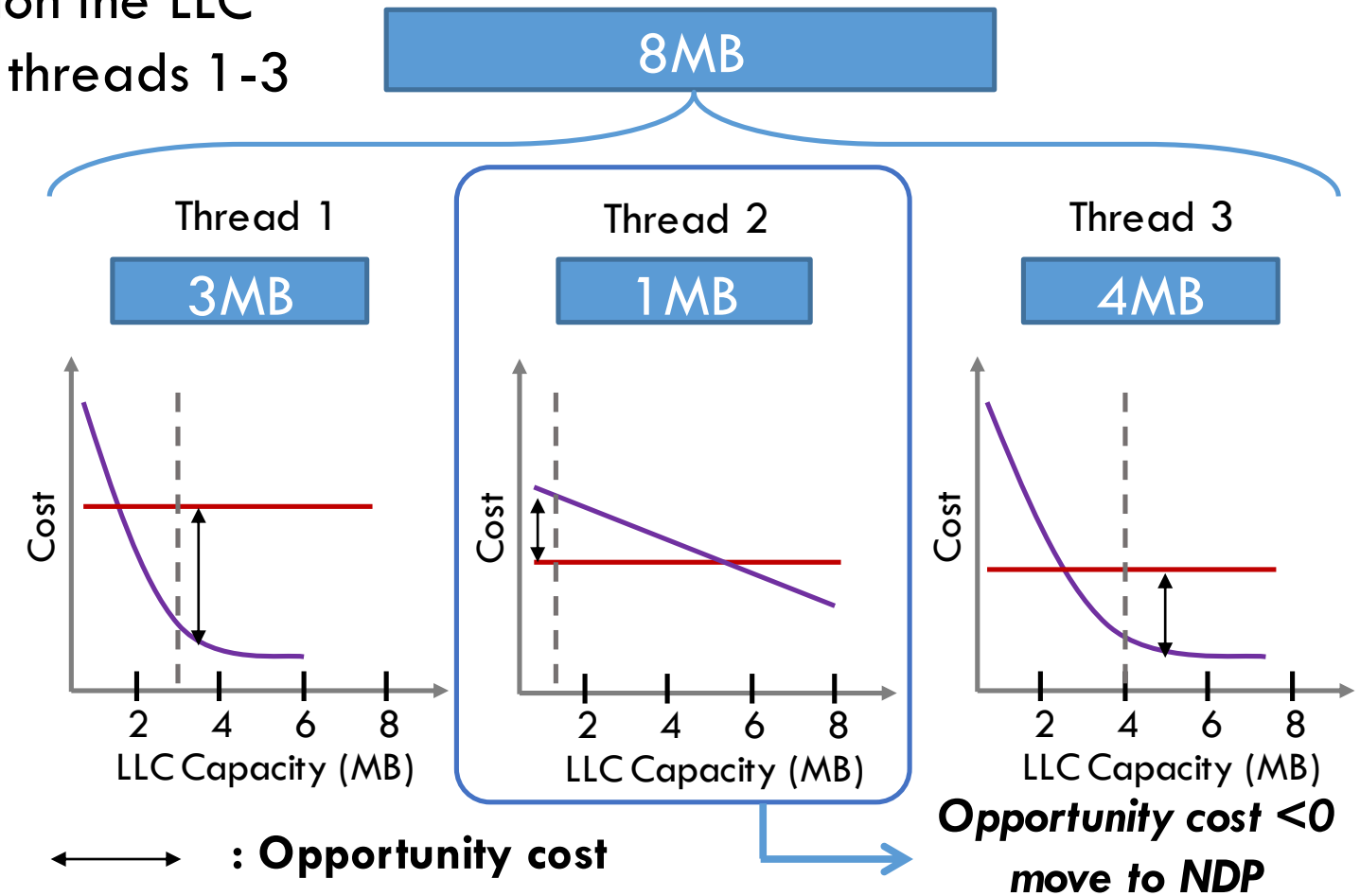
Partition the LLC among threads 1-3



Perform multiple rounds of partitioning until the processor die is not oversubscribed

Overhead: 0.1% of system cycles when scheduling every 50ms

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- AMS-DP serves as the upper bound of AMS-Greedy
  - But it is more expensive

Data placement for asymmetric hierarchies

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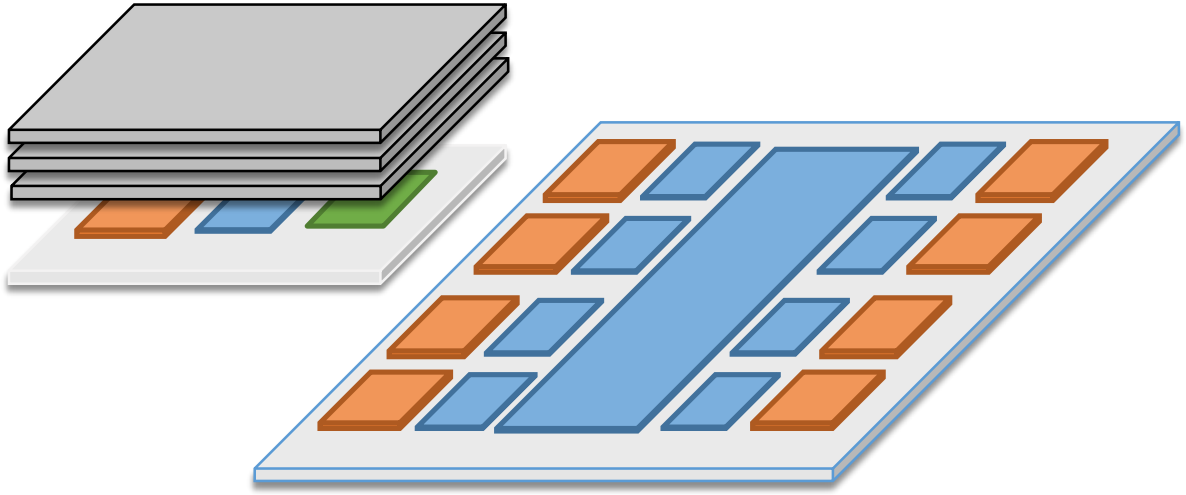

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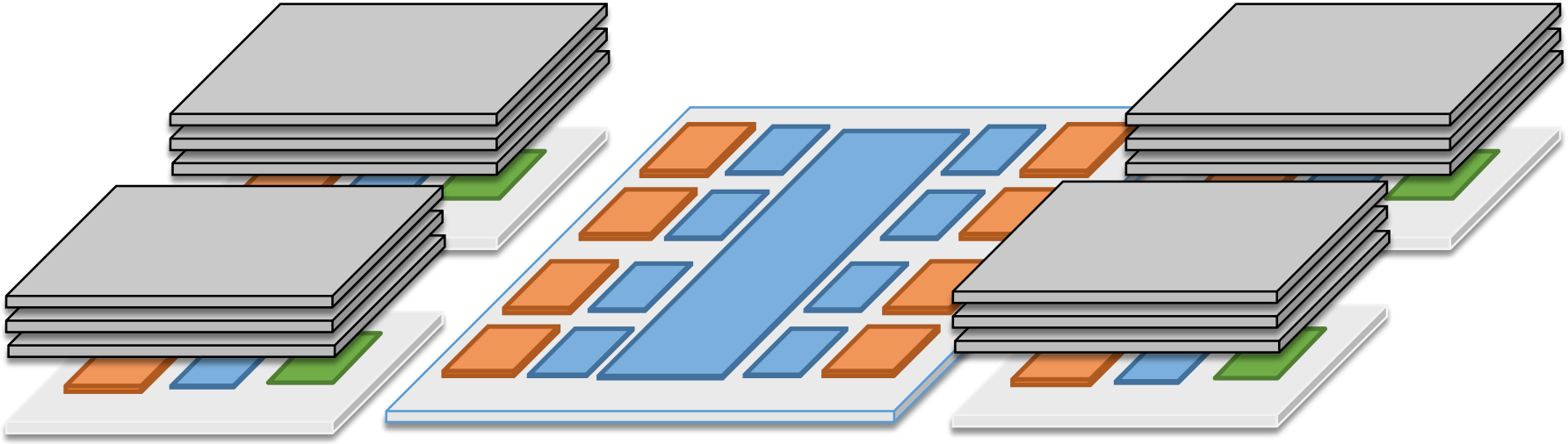
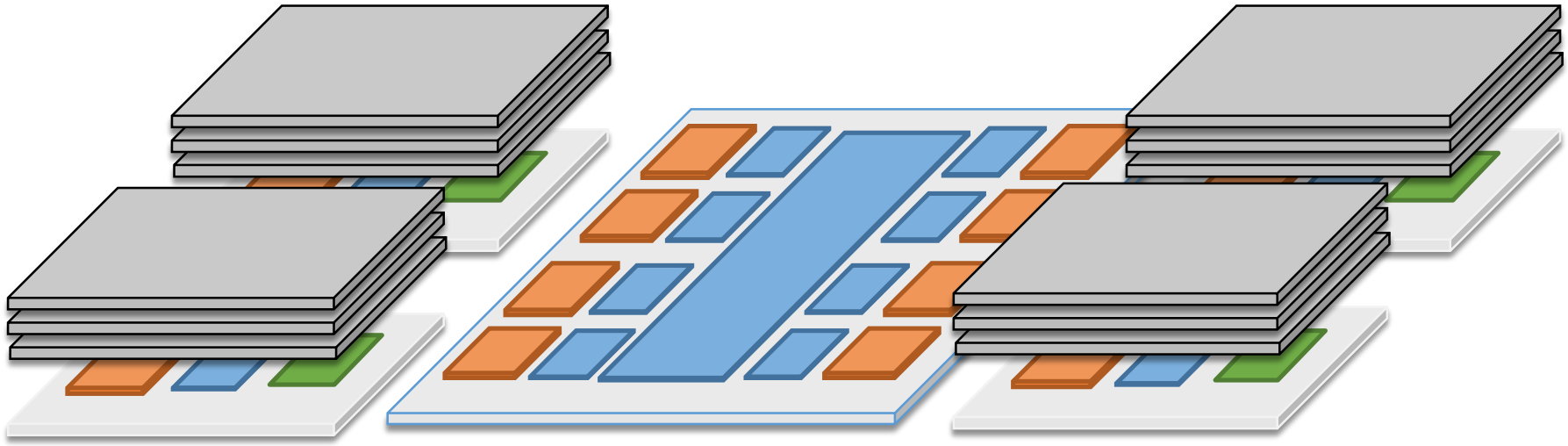


Data placement for asymmetric hierarchies

- NDP systems have different constraints from NUMA systems
  - NDP cores have plentiful intra-stack bandwidth but limited inter-stack bandwidth



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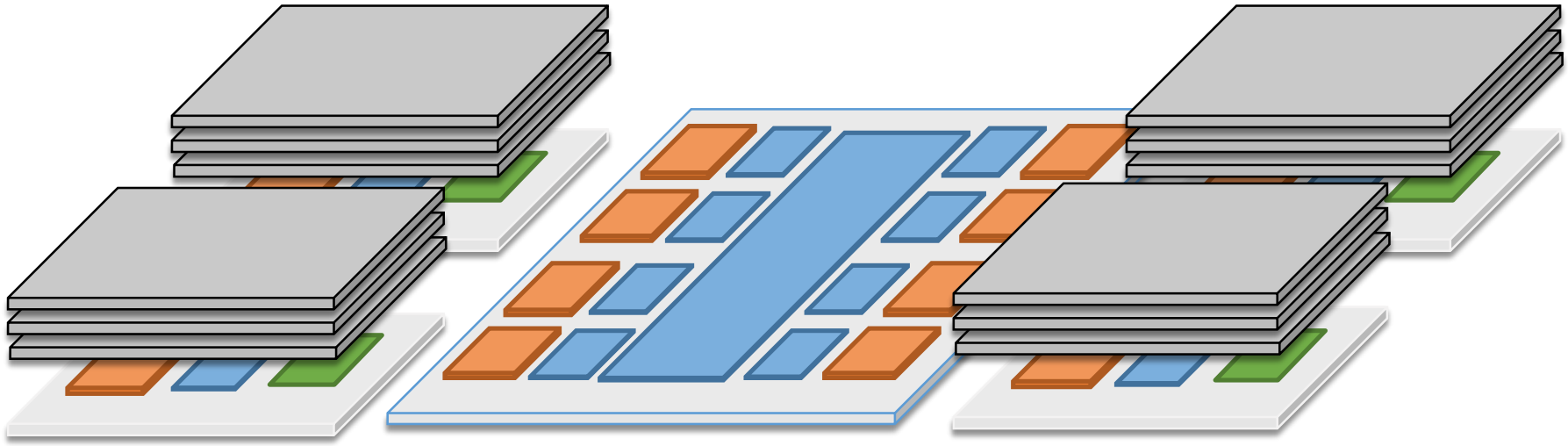
- We use simple heuristics to keep data from a thread in a single stack
  - Threads try to allocate to the same stack so long as the stack has enough capacity



See paper for more details

- Handling multithreaded workloads
- AMS-DP formulation
- Different system scenarios
  - Oversubscribed systems
  - Short-lived workloads or latency critical workloads

Evaluation

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- Modeled system:

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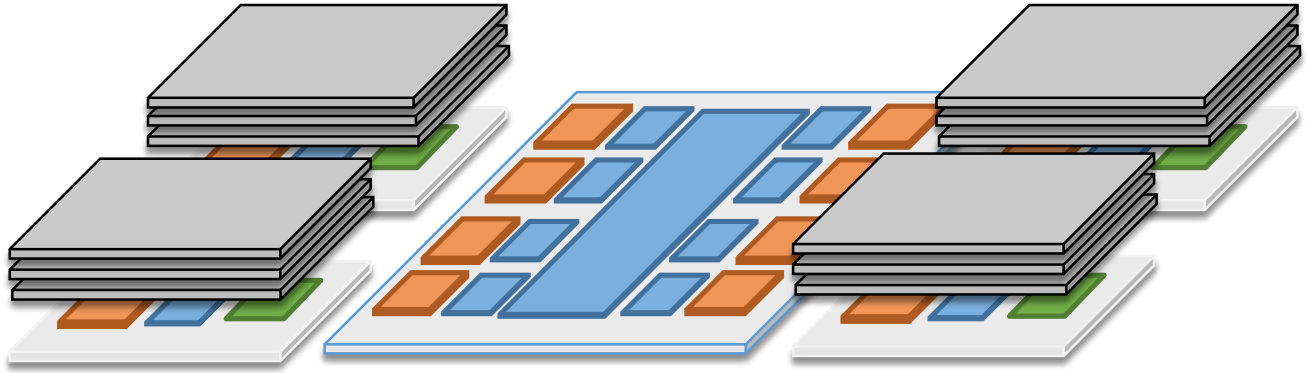

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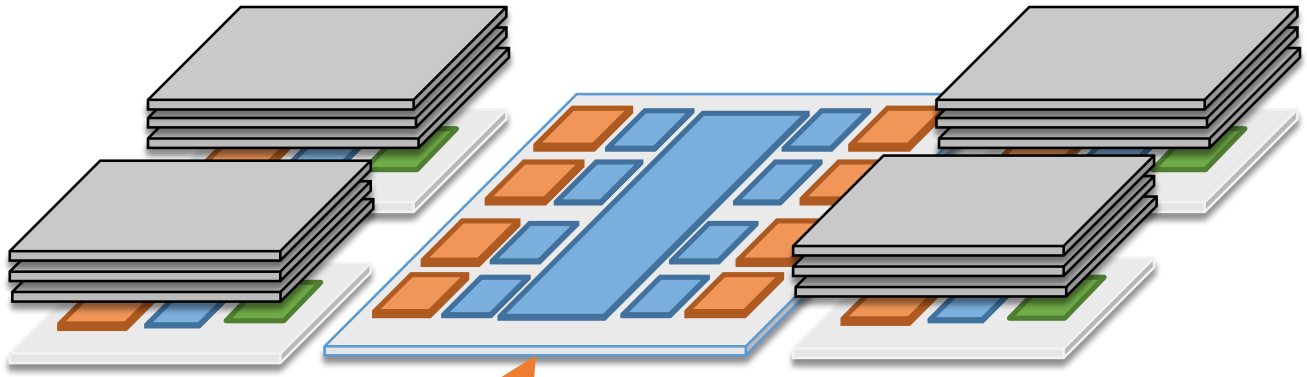

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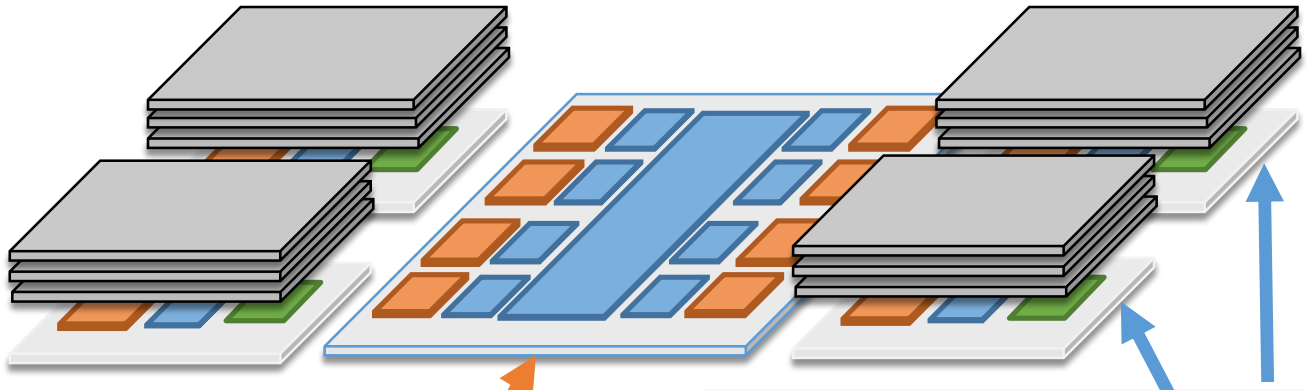

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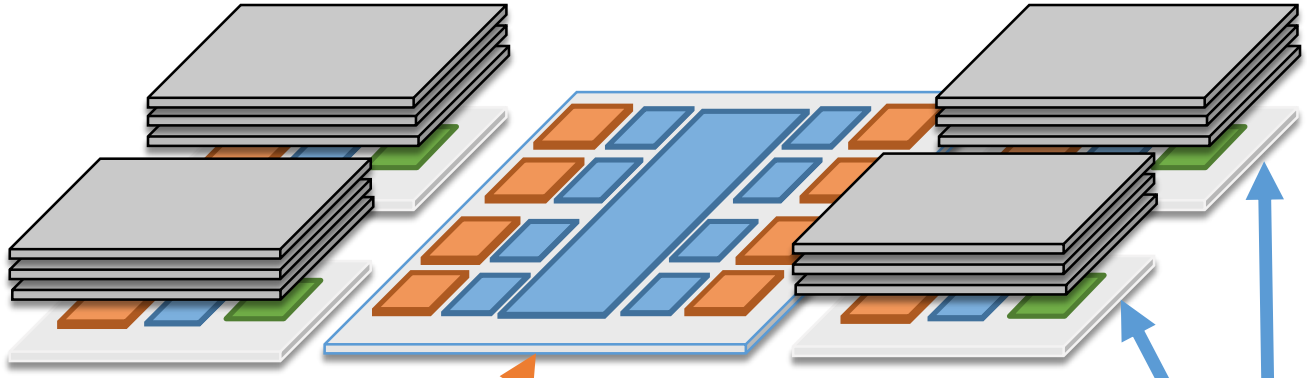

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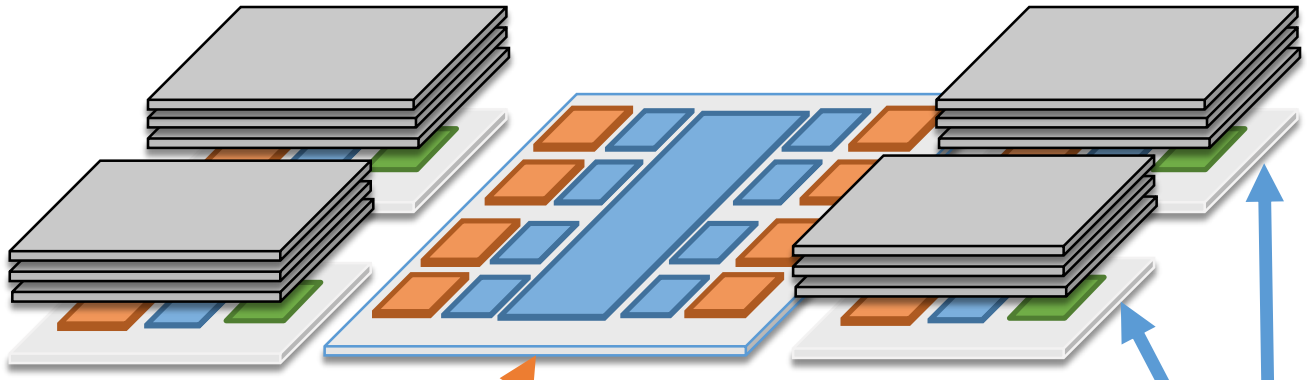

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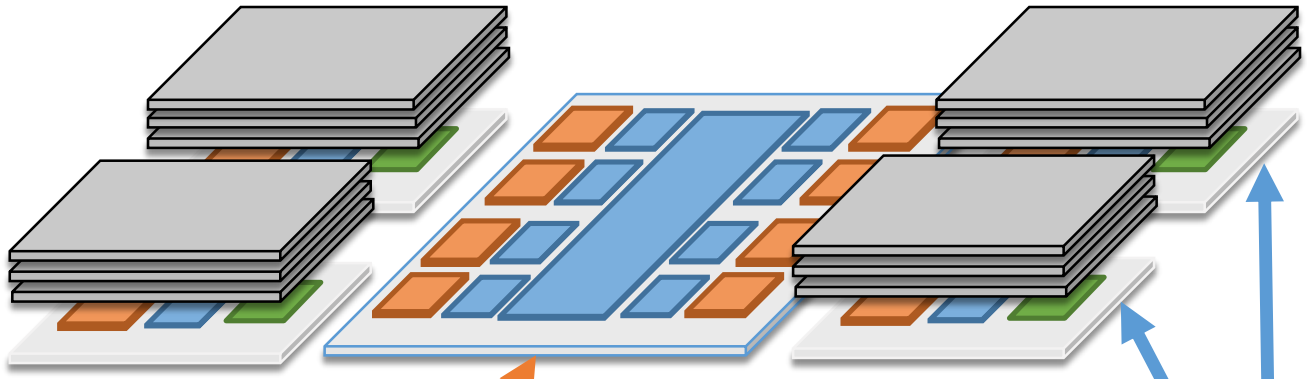

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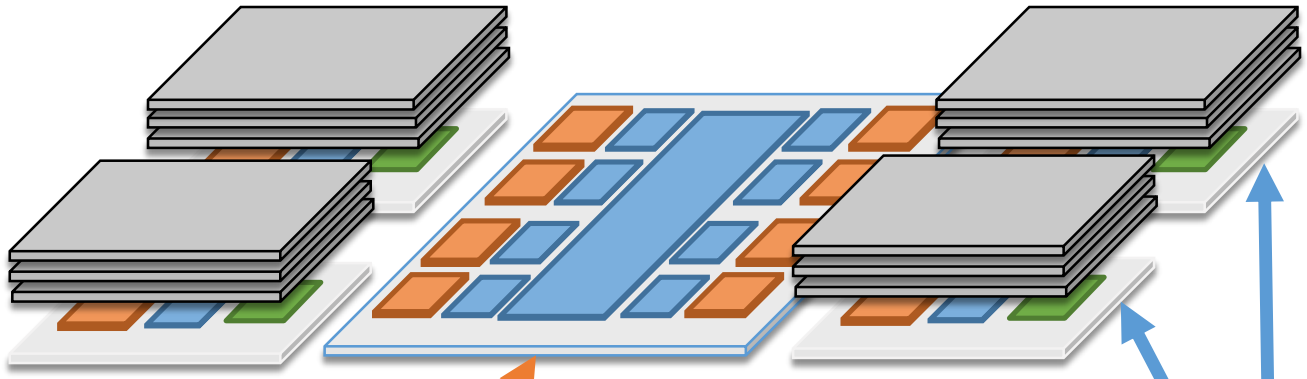

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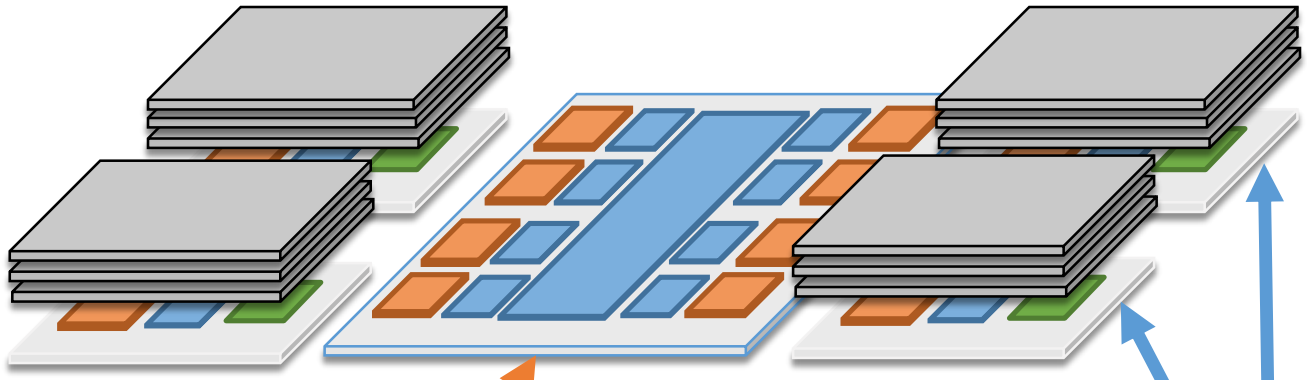

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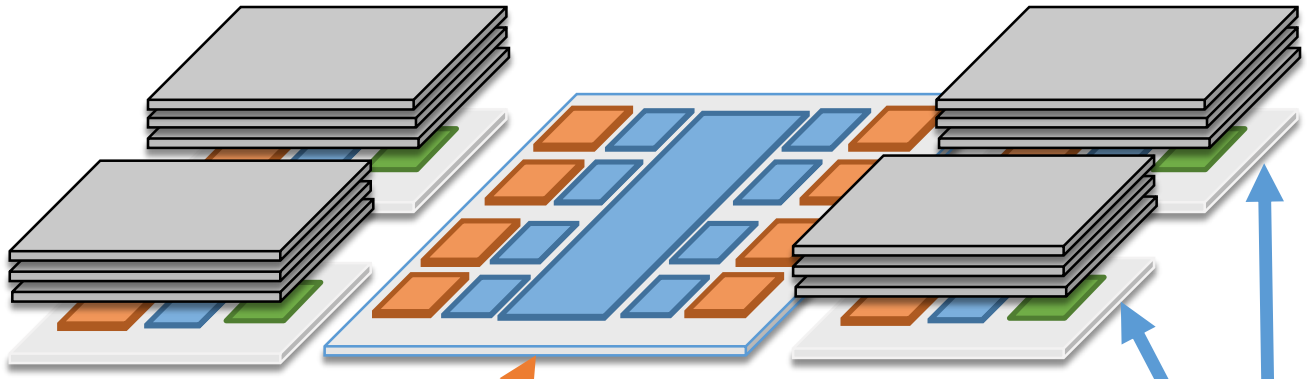

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  - AMS-Greedy/AMS-DP

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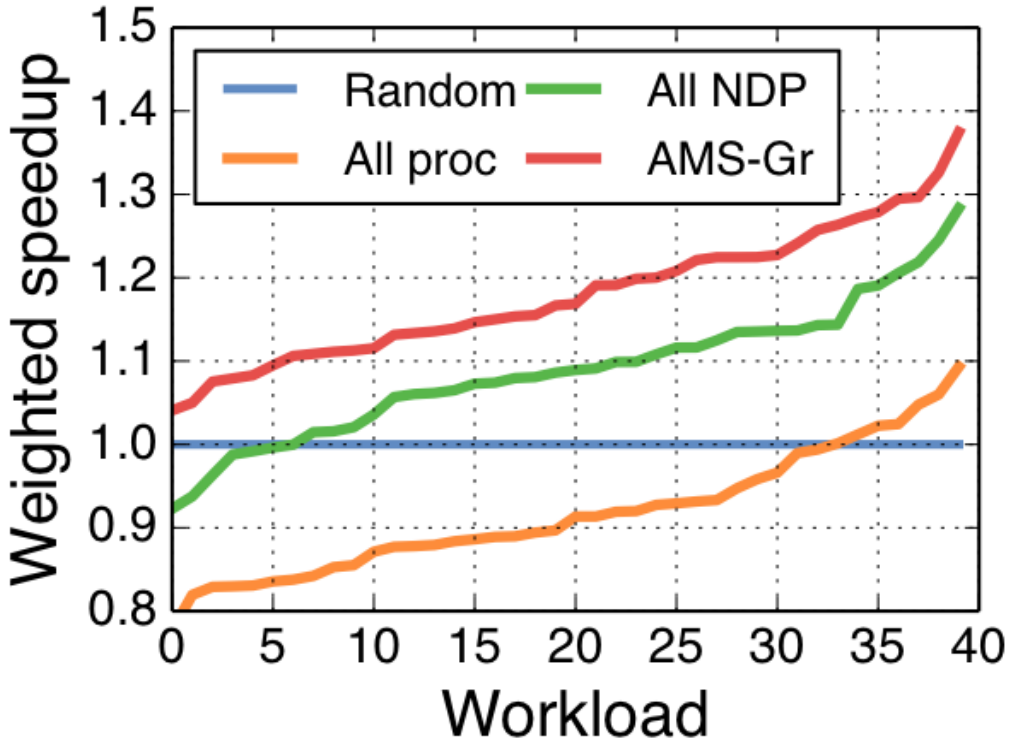

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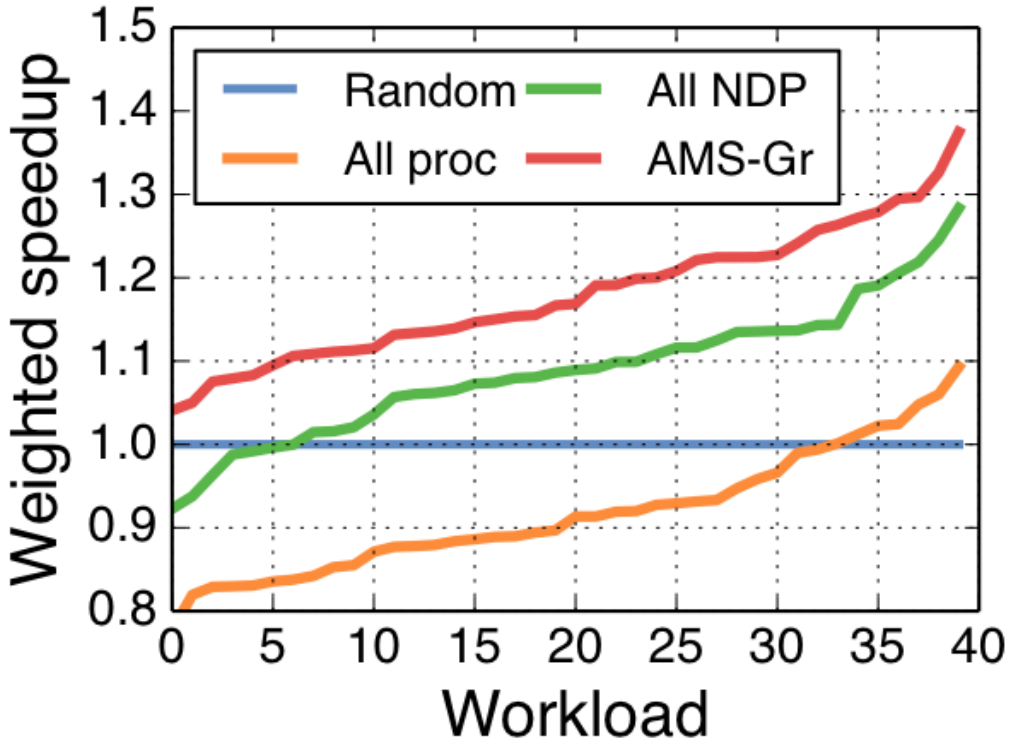

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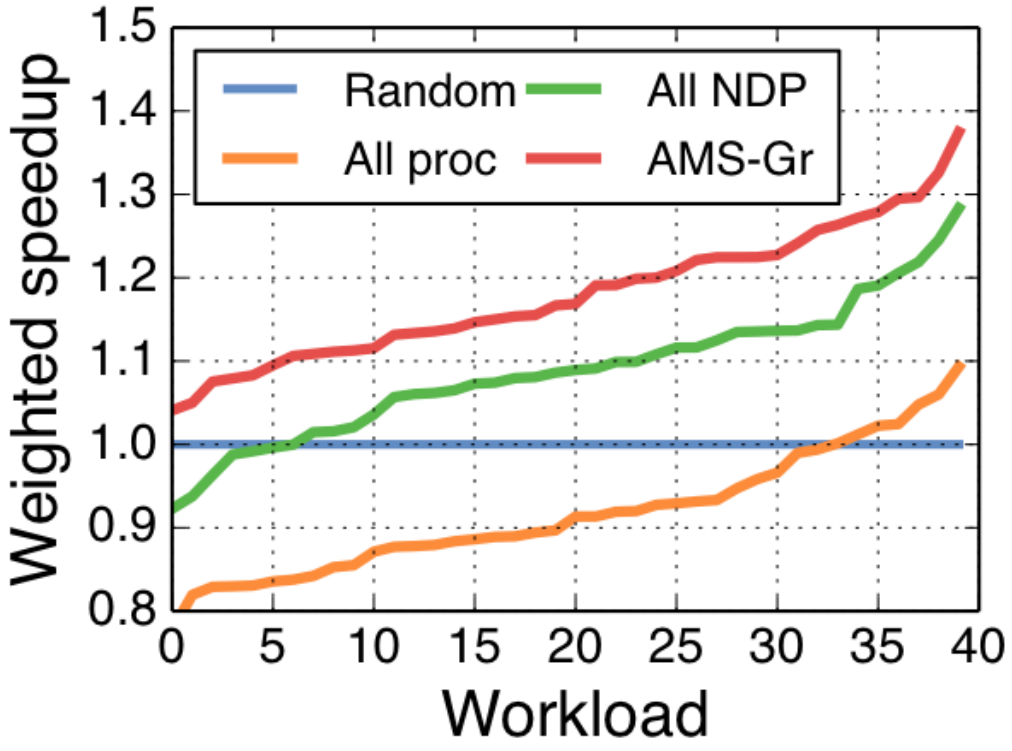

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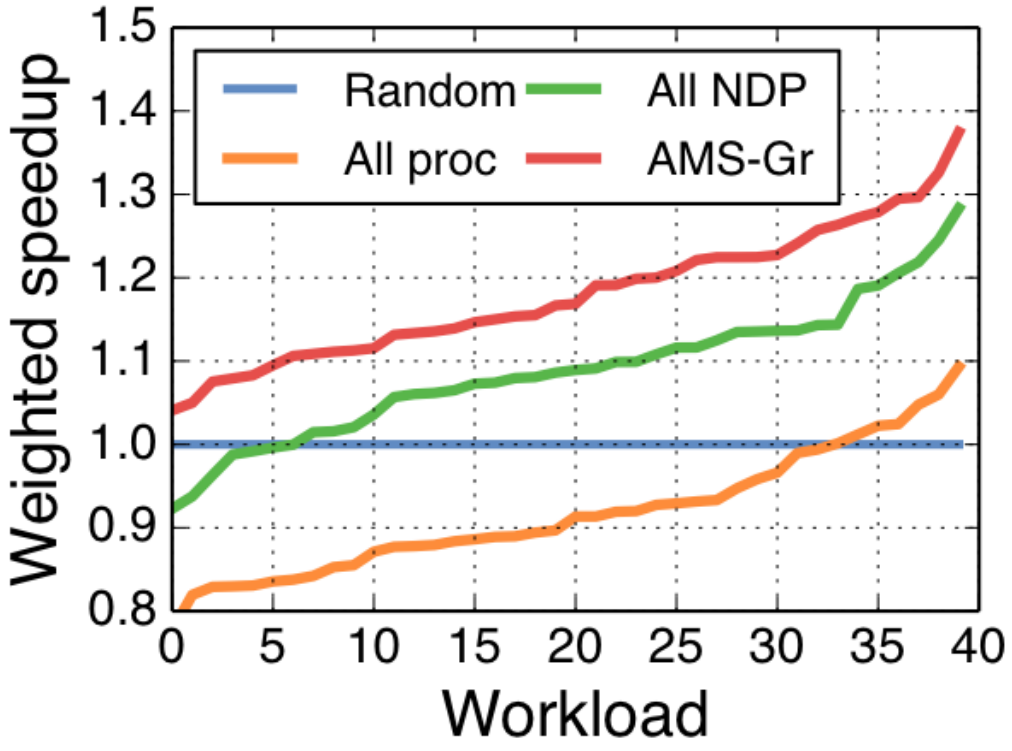

AMS-Greedy never hurts performance and improves weighted speedup by up to 37% and by 18% on average

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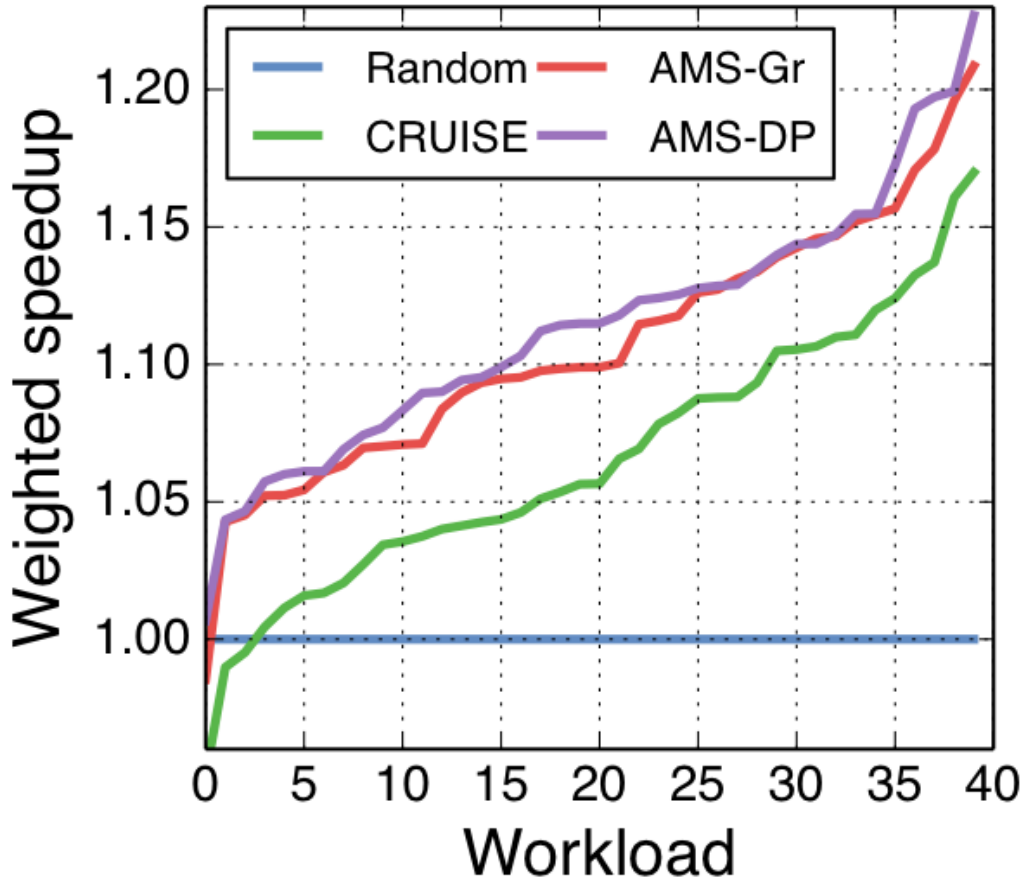

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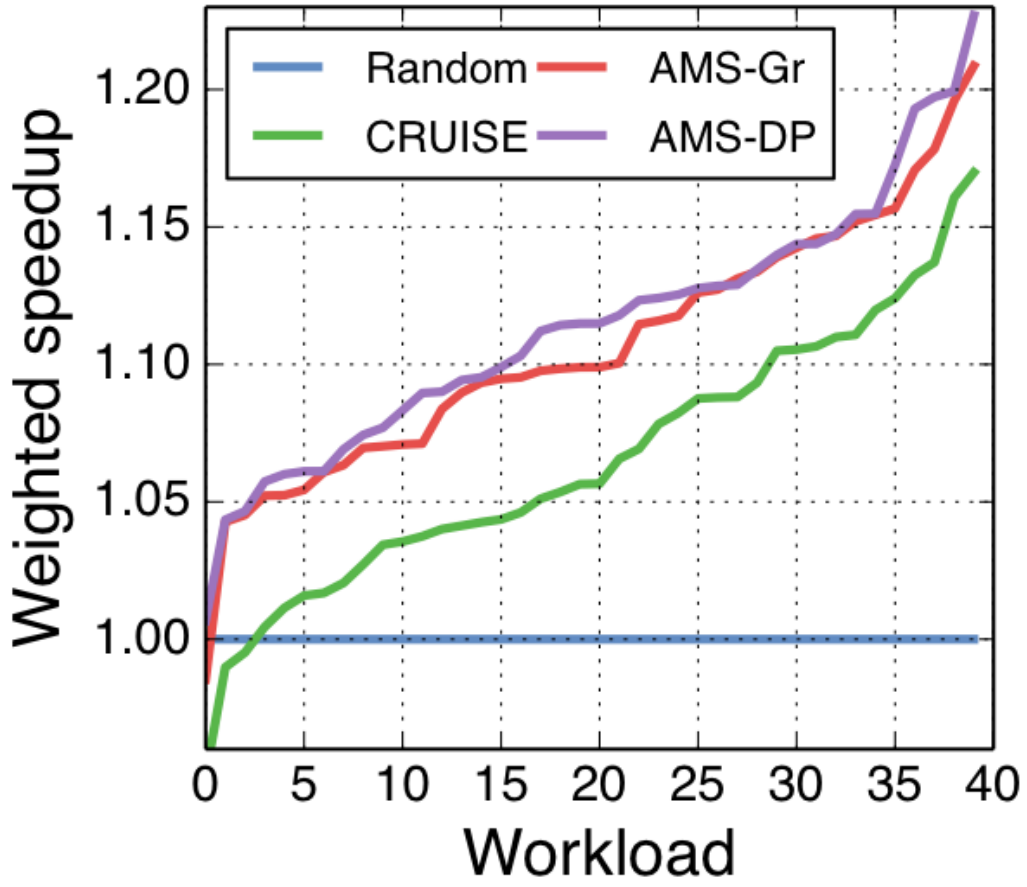

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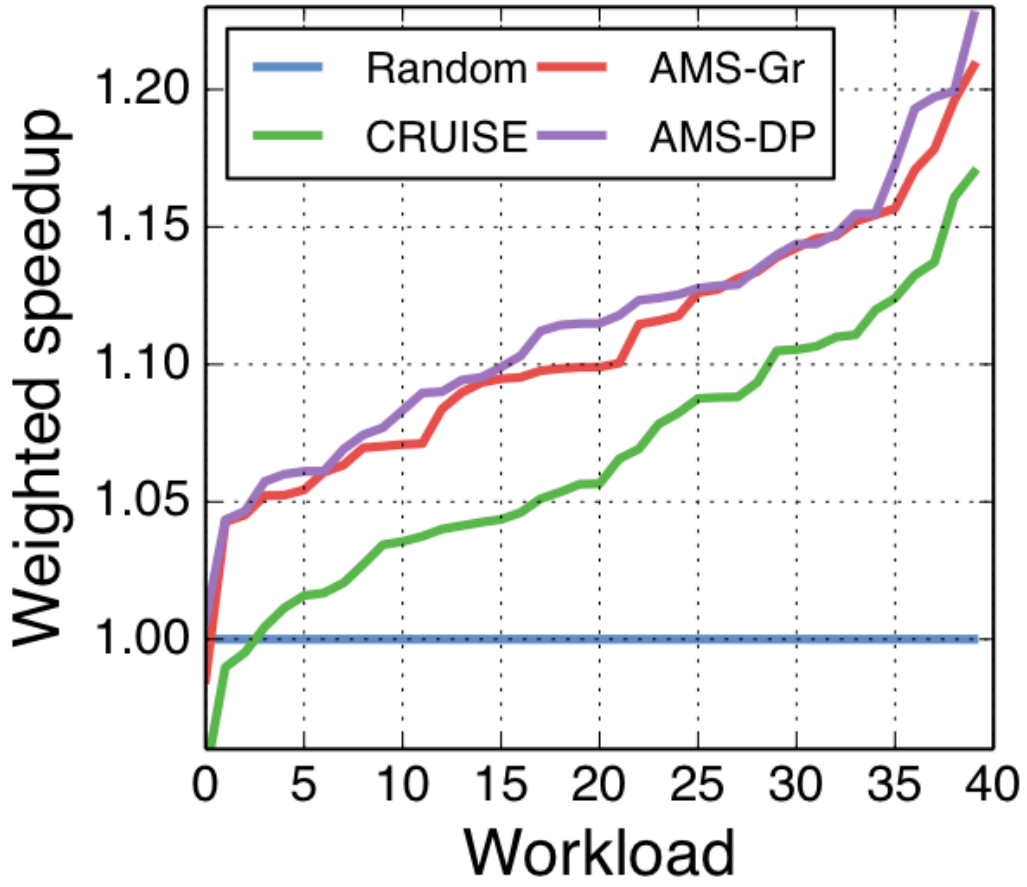

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Both AMS-Greedy and AMS-DP outperform CRUISE

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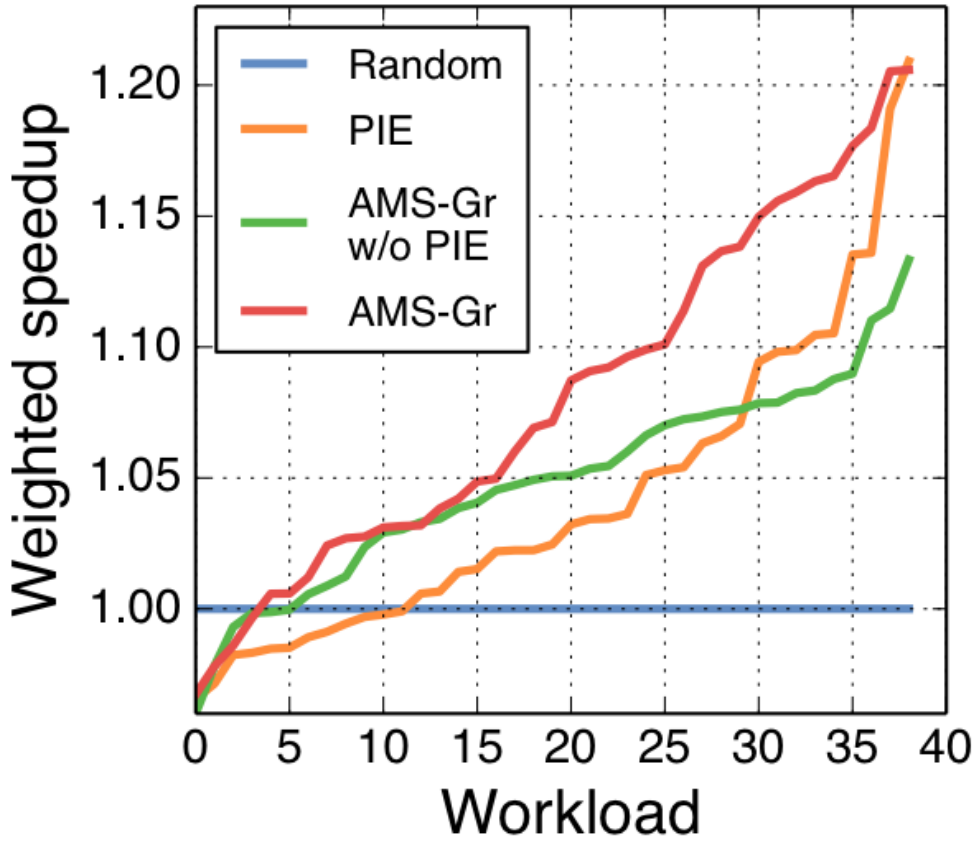

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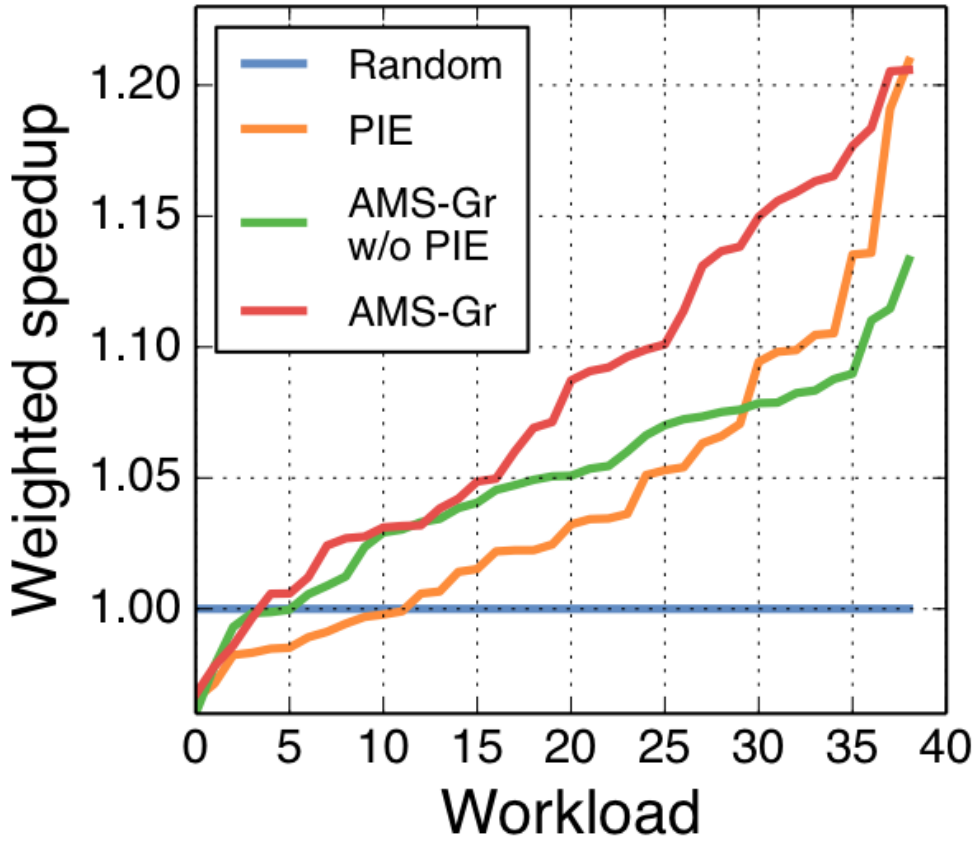

AMS-Greedy with the PIE model improves performance more than handling core/memory asymmetries separately

See paper for more evaluation results

- A case study to show AMS adapts to application phases
- Multithreaded workloads
- Detailed runtime overheads
- Sensitivity study for system parameters
  - Number of cores, LLC capacity, main memory capacity
  - Performance without and with hardware support for cache partitioning

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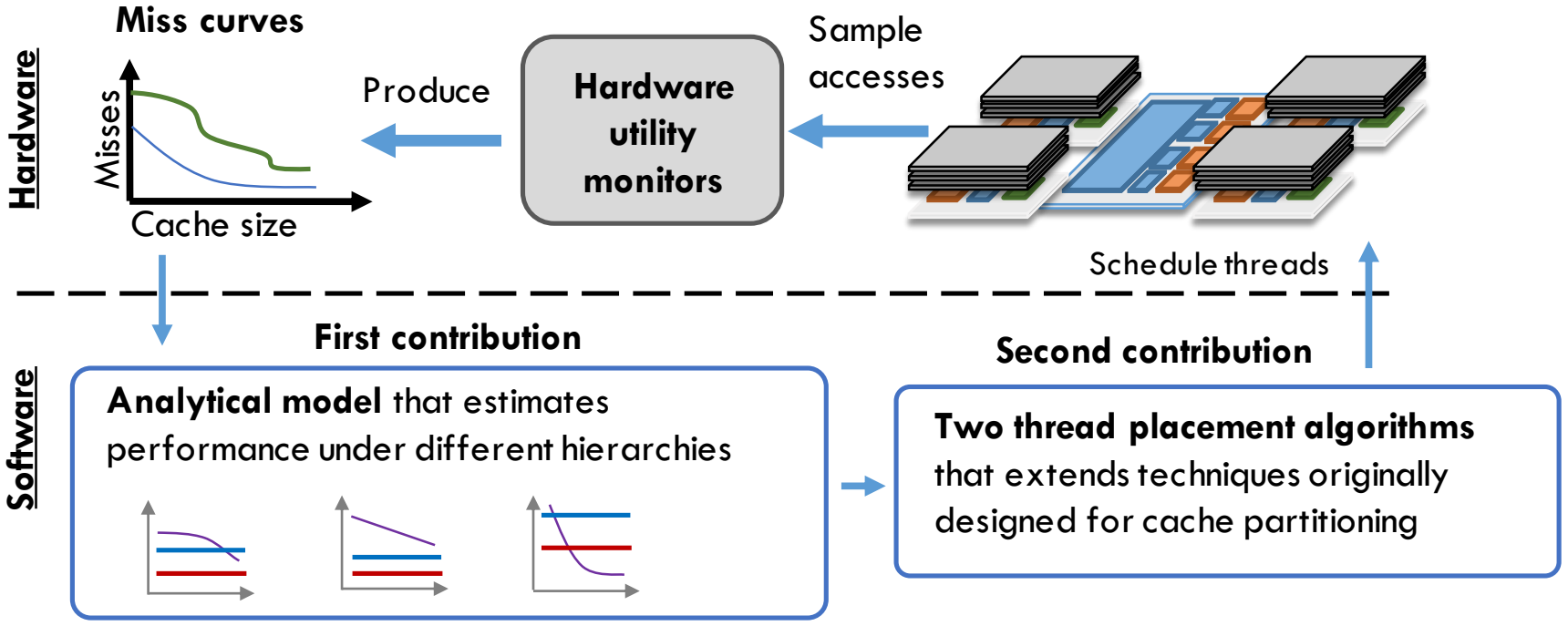

Thanks! Any questions?

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