PHI: ARCHITECTURAL SUPPORT FOR SYNCHRONIZATION- AND BANDWIDTH-EFFICIENT COMMUTATIVE SCATTER UPDATES

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MICRO 2019

Carnegie Mellon University

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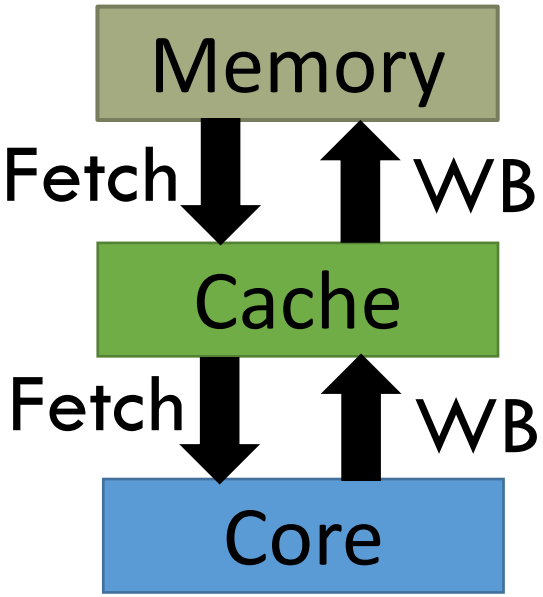

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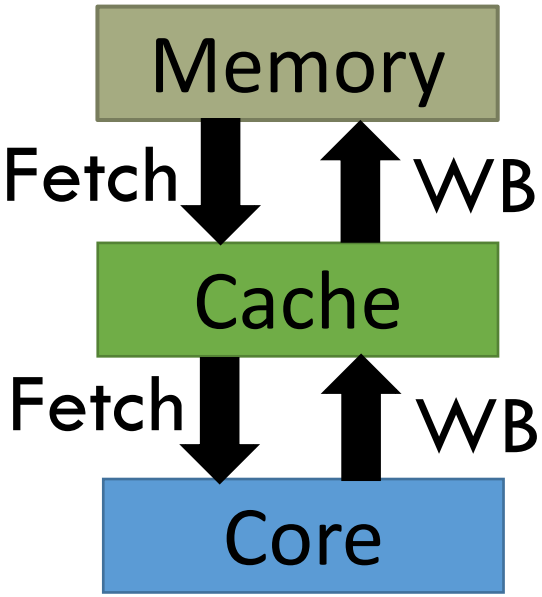

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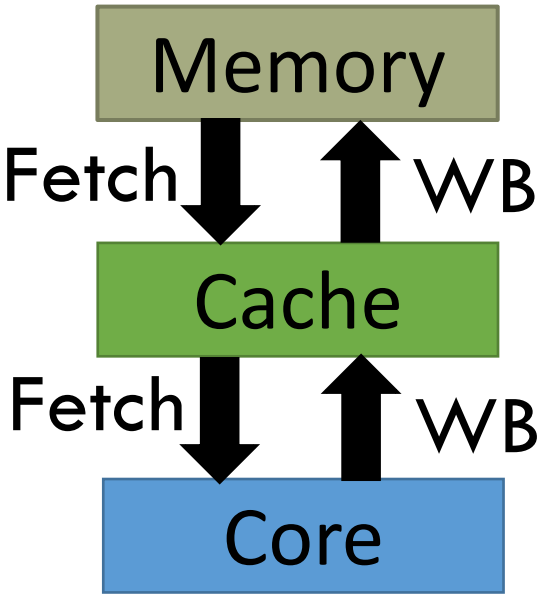

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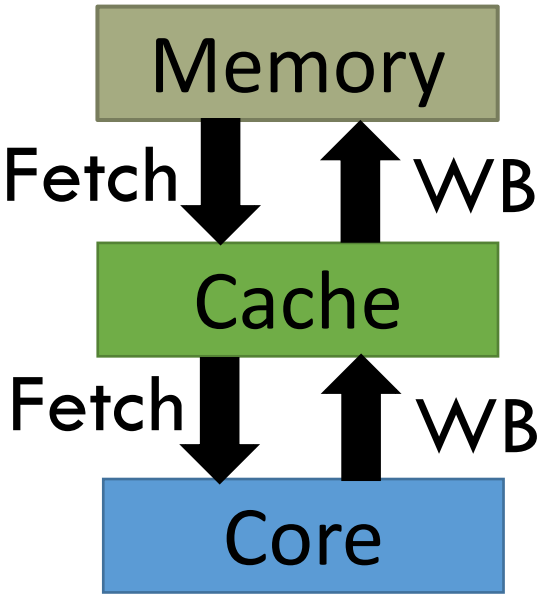

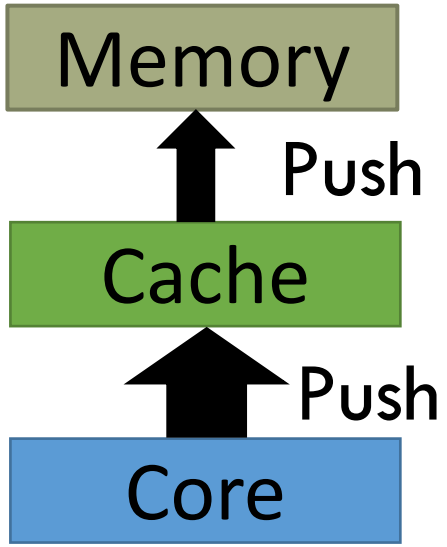

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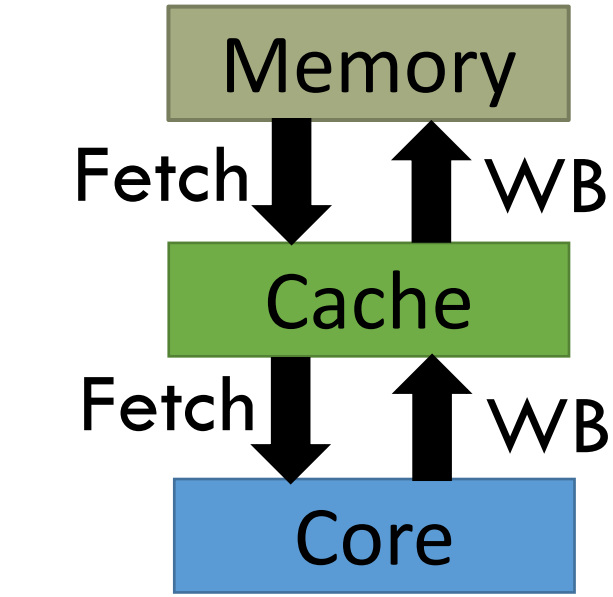

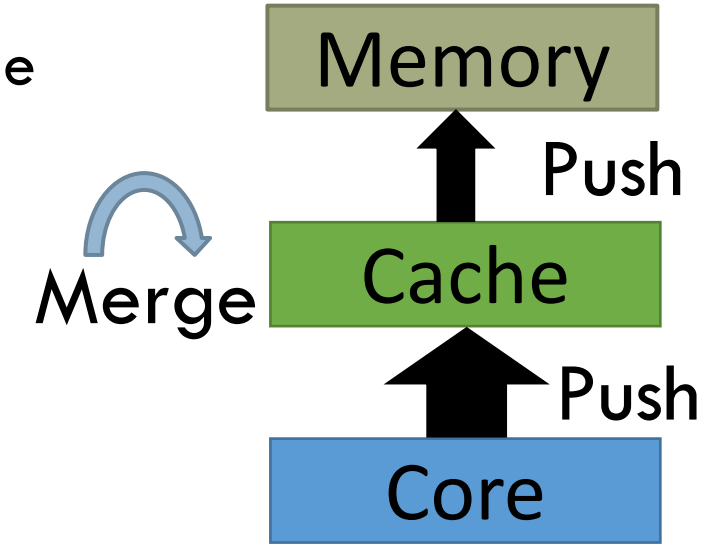

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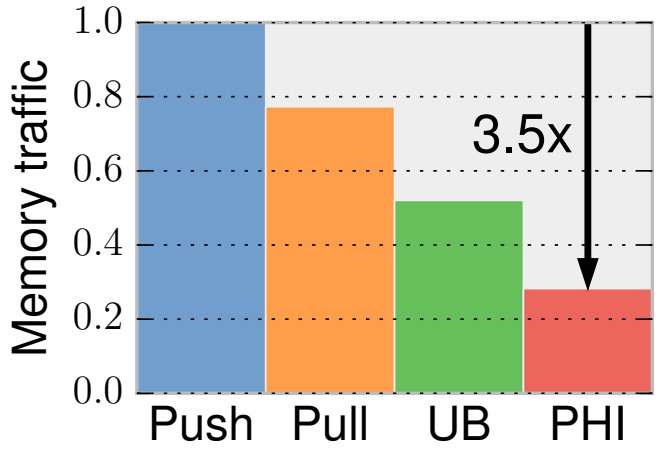

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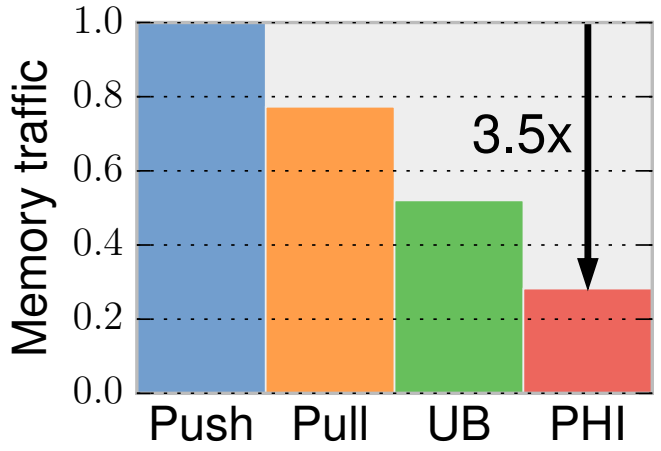

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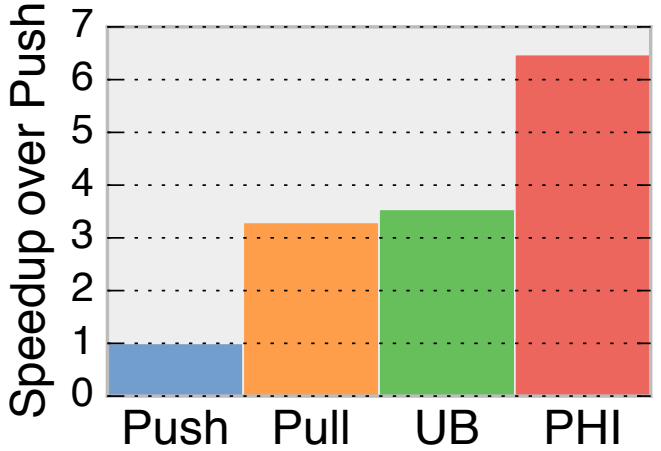

Performance

Agenda

- **Background**
- PHI Design
- Evaluation

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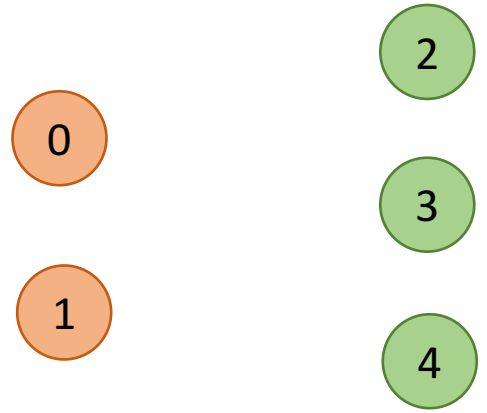

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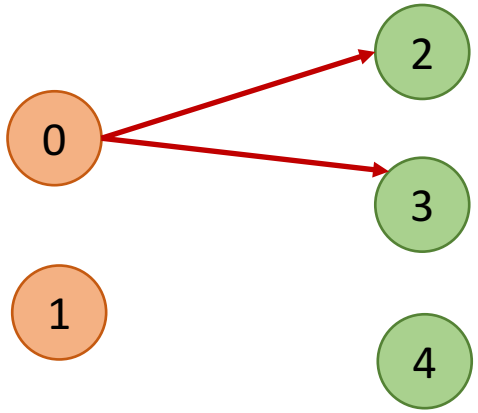

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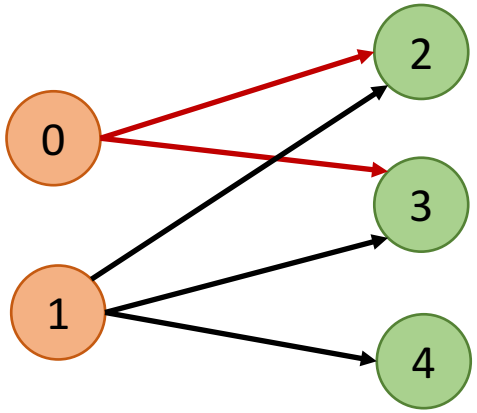

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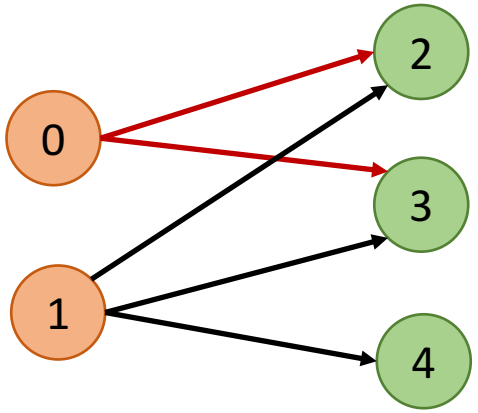

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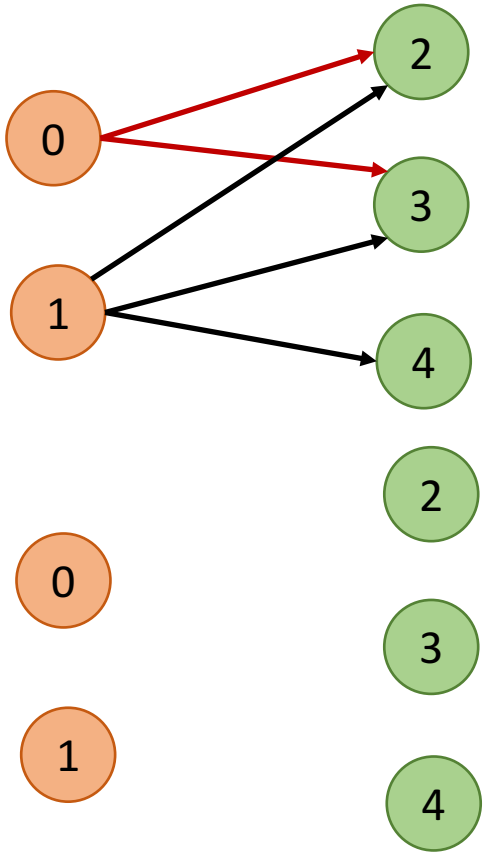

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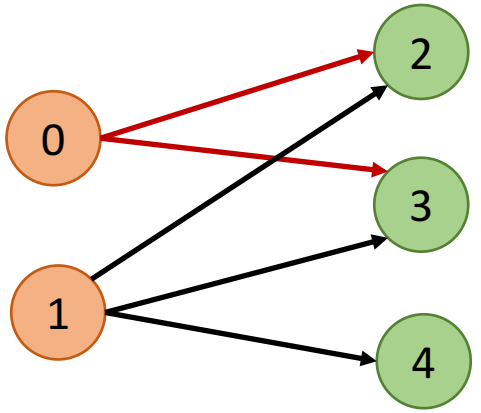

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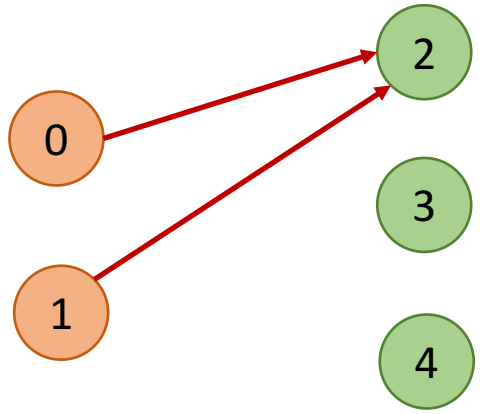

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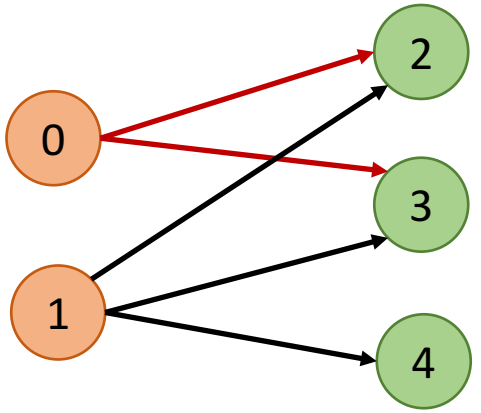

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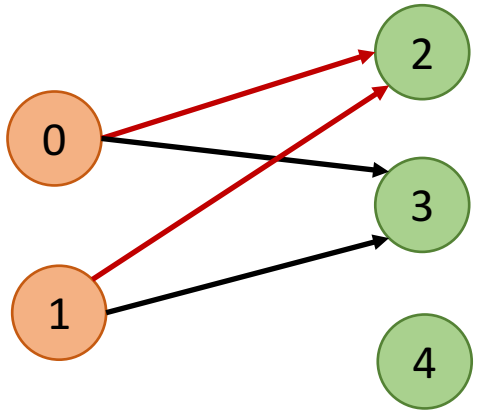

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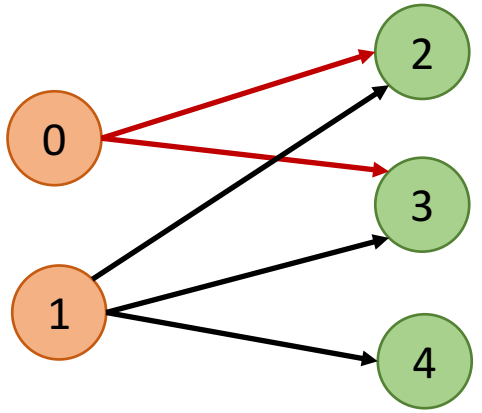

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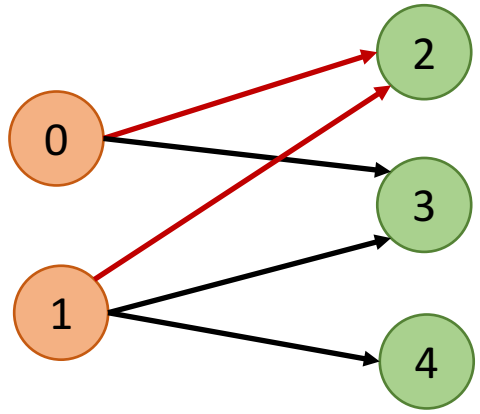

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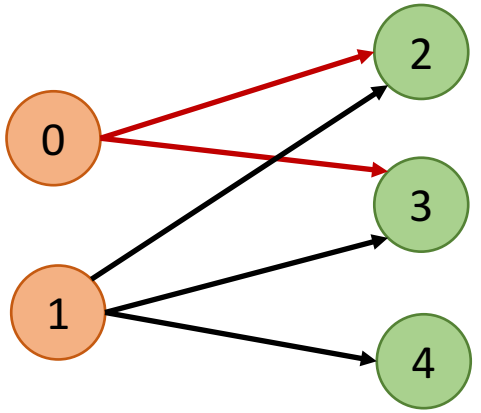

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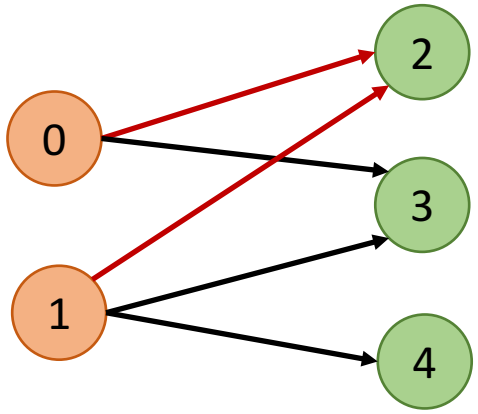

- Important to support scatter updates efficiently
  - Push mode performs less work when few vertices are active
  - Some algorithms do not admit a pull implementation

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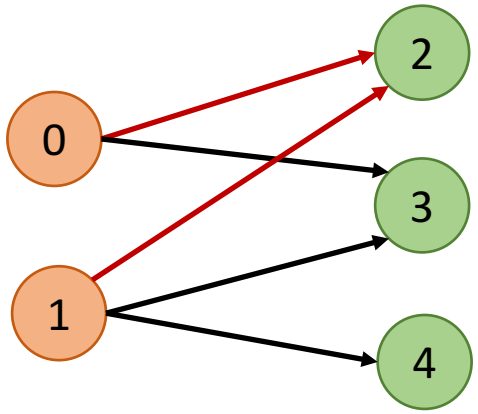

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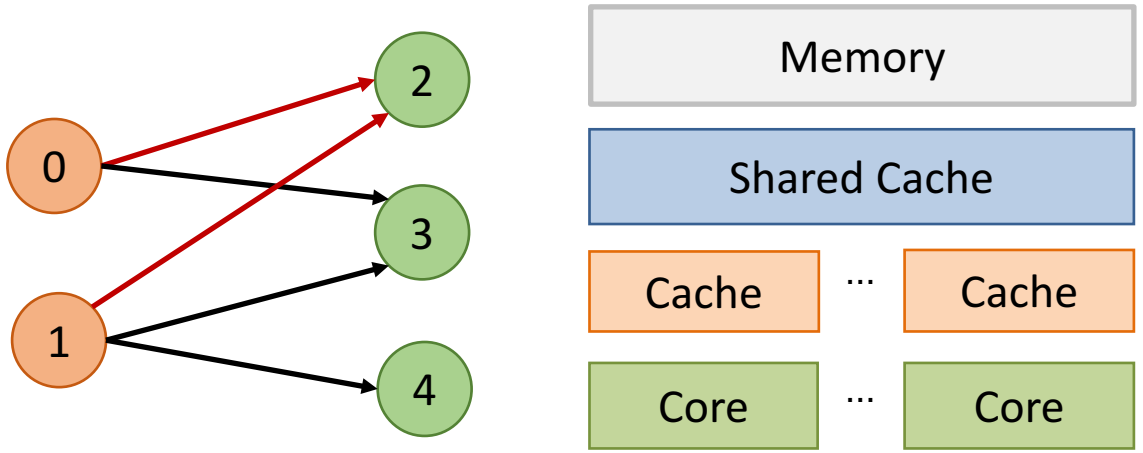

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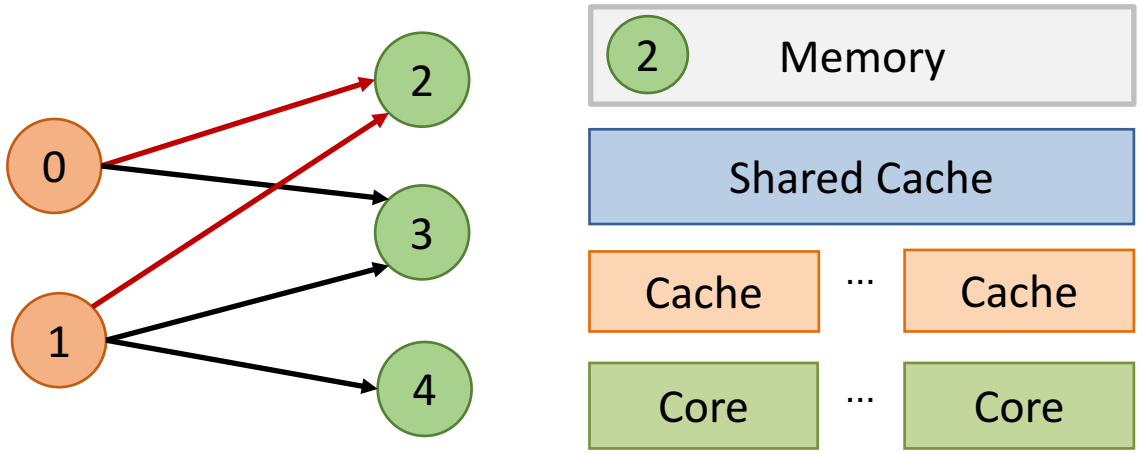

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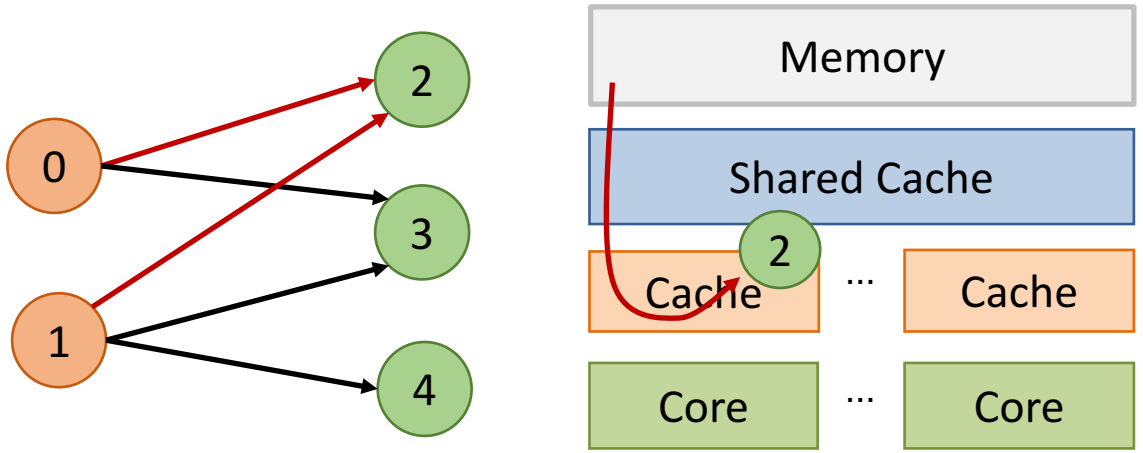

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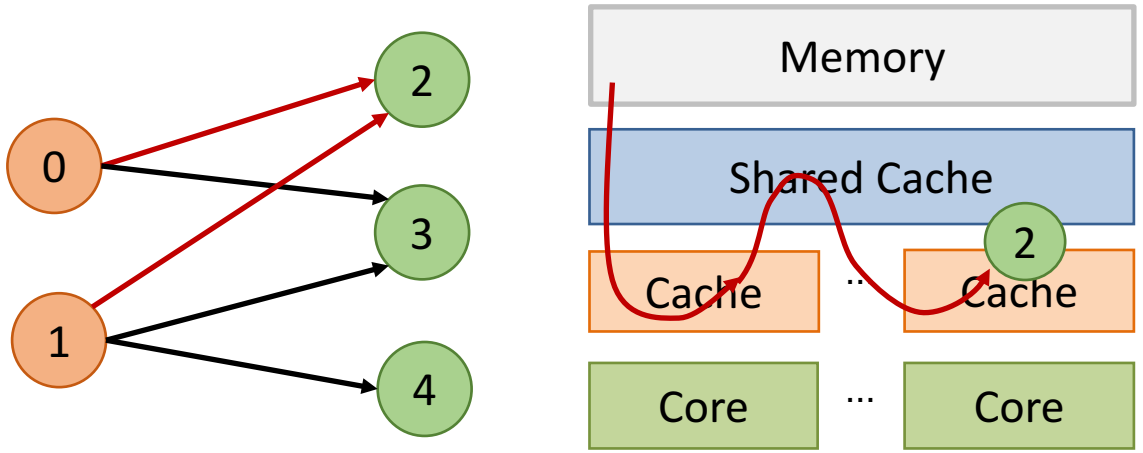

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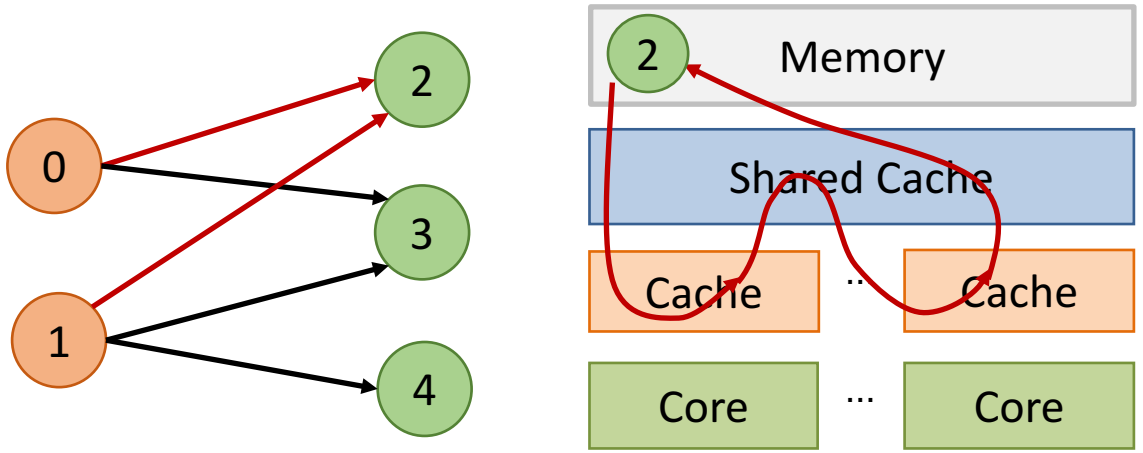

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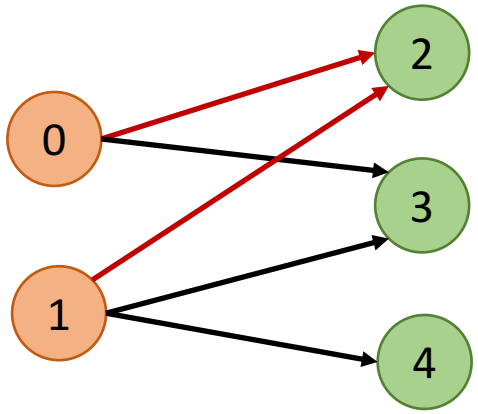
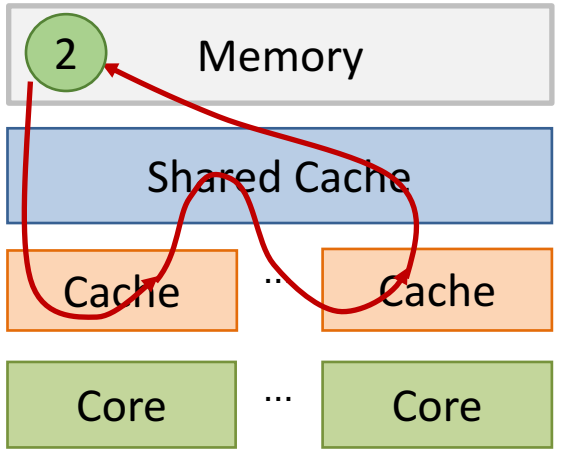
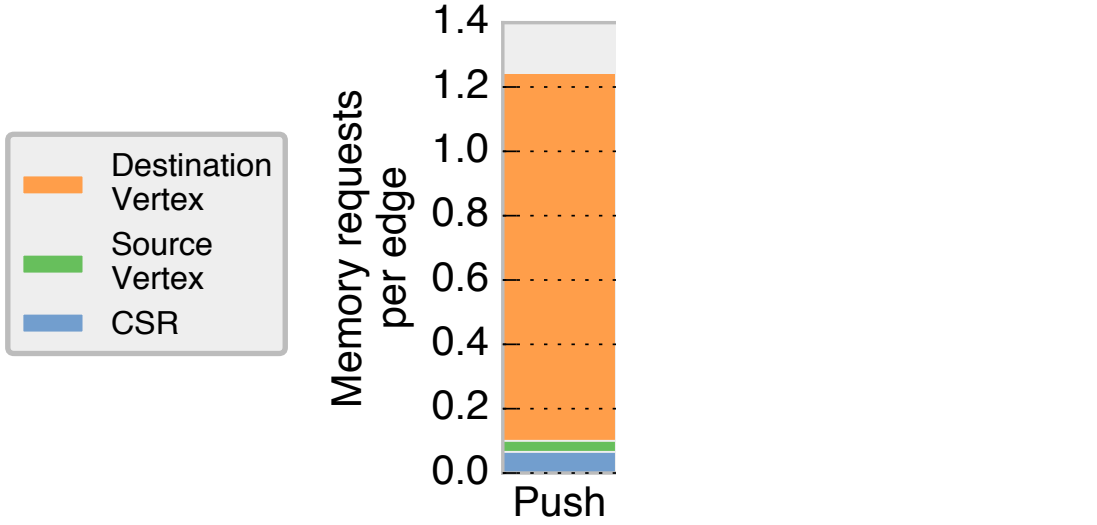




Push PageRank on uk-2005 graph



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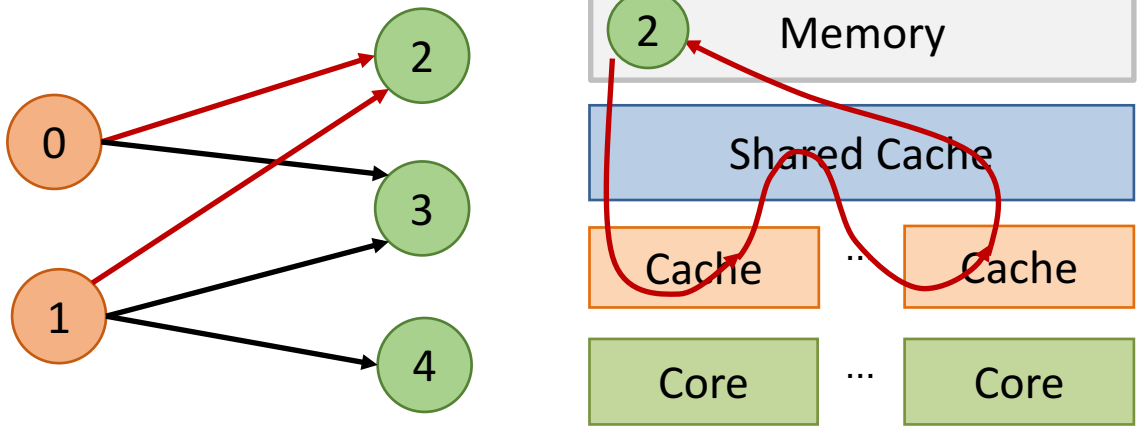

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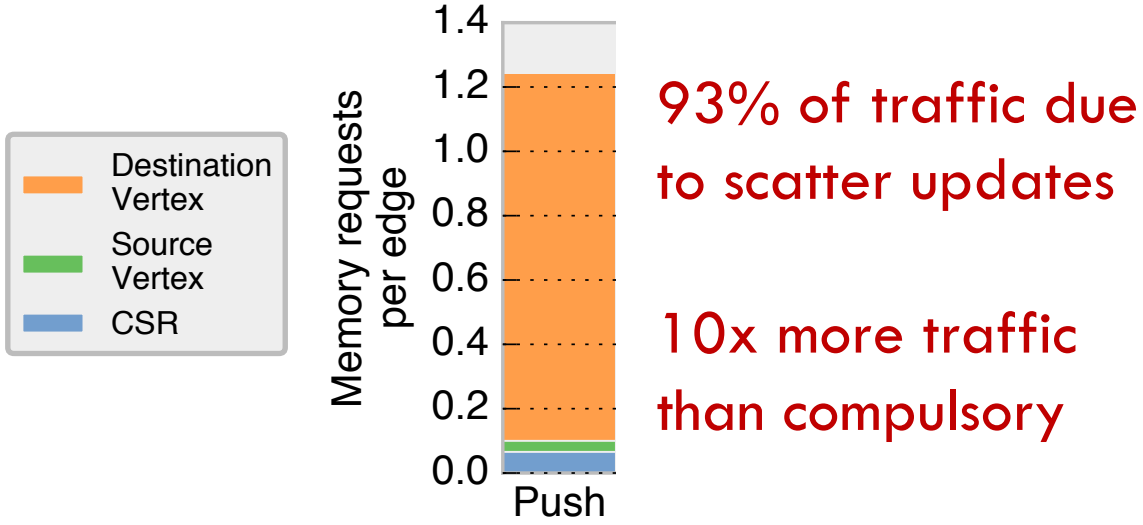

93% of traffic due to scatter updates

10x more traffic than compulsory

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- Both RMOs and COUP do not improve locality
  - Bottlenecked by memory traffic with large inputs

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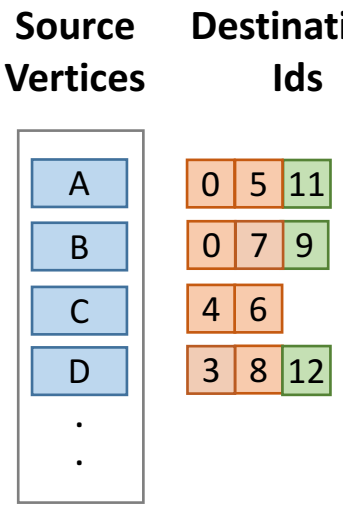

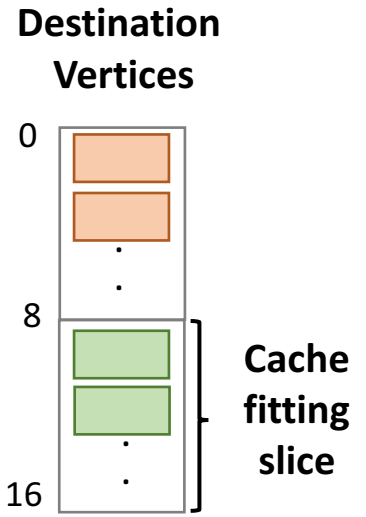

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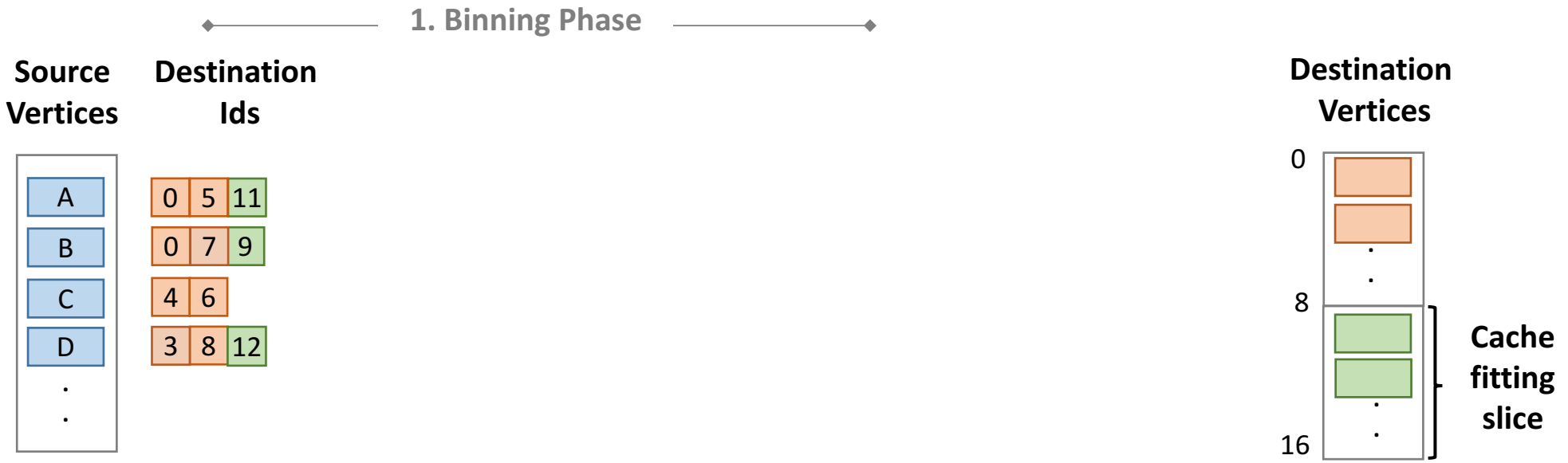

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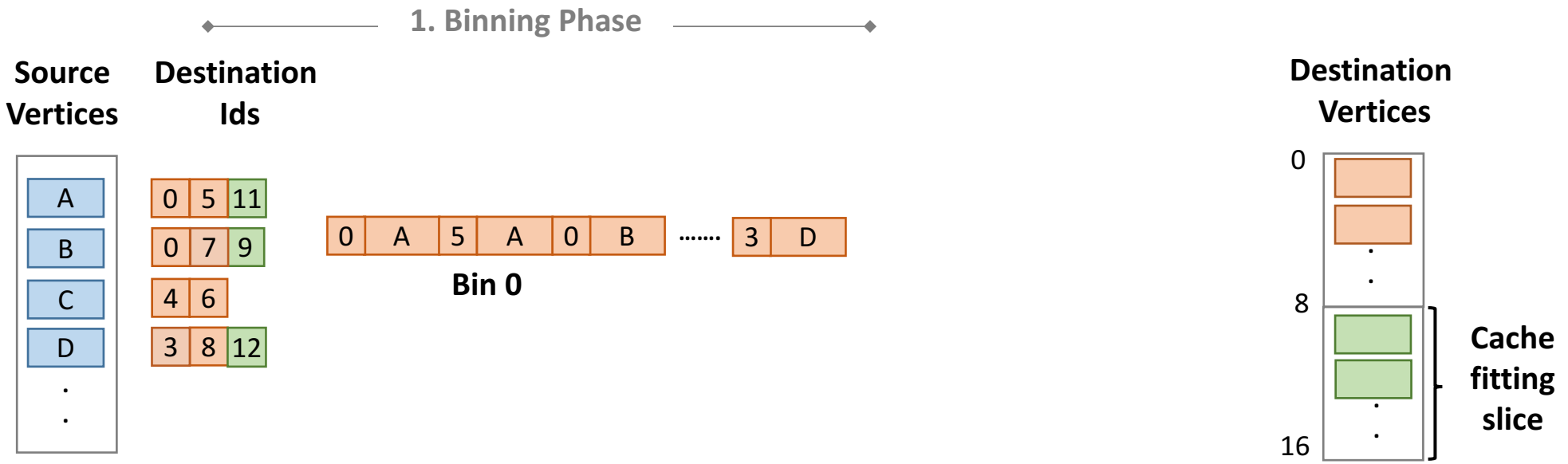

Propagation Blocking [*IPDPS'17*], MILK [*PACT'16*]

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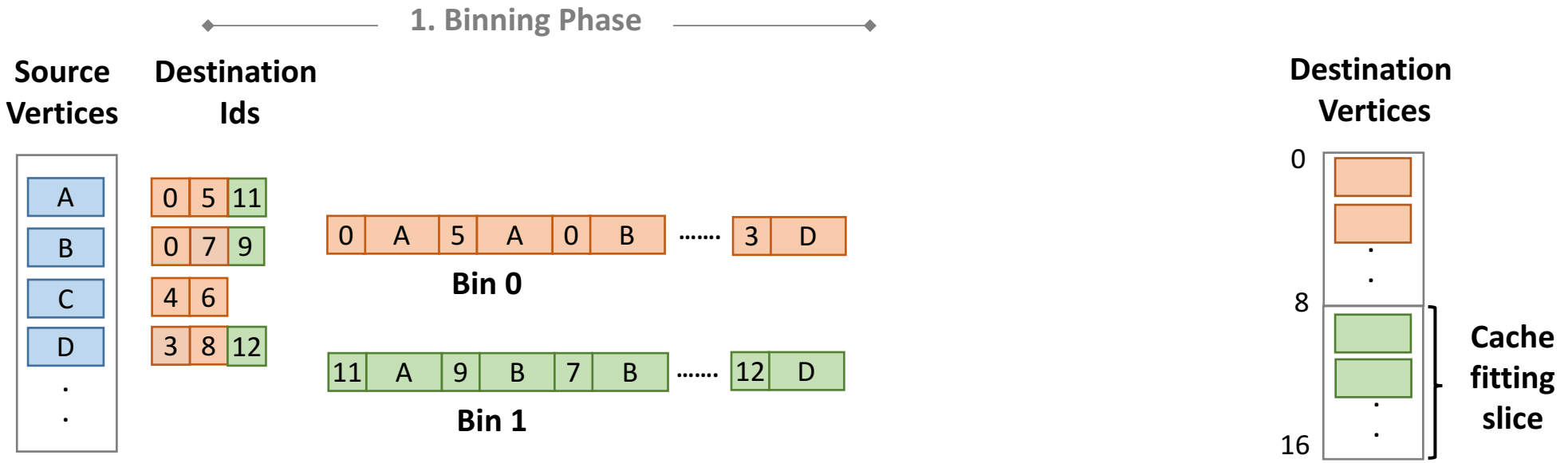

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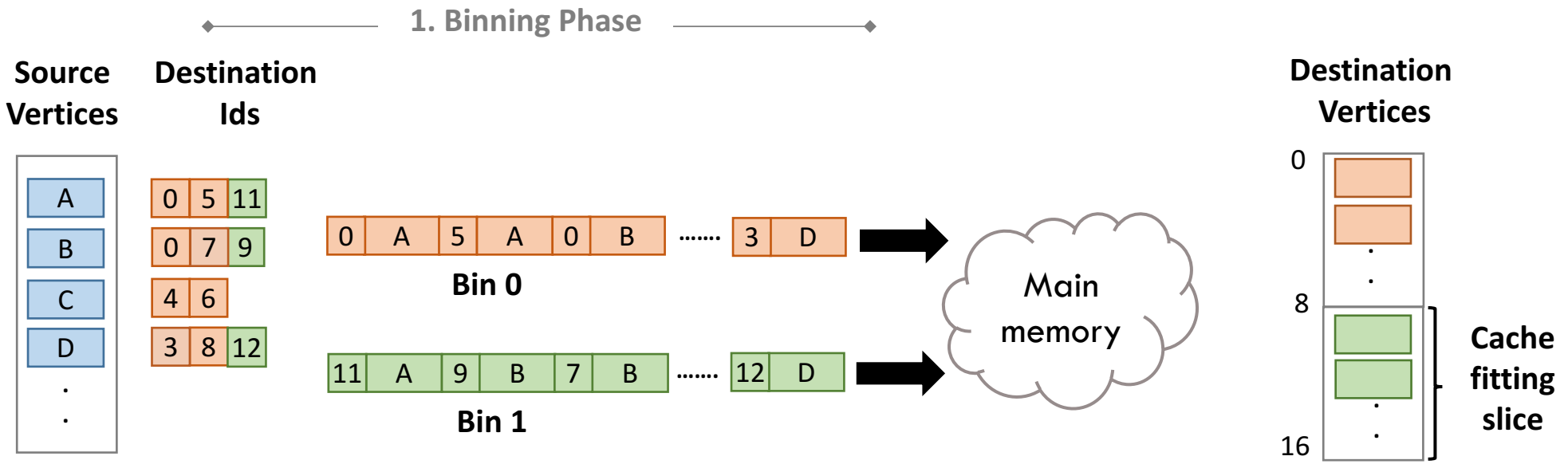

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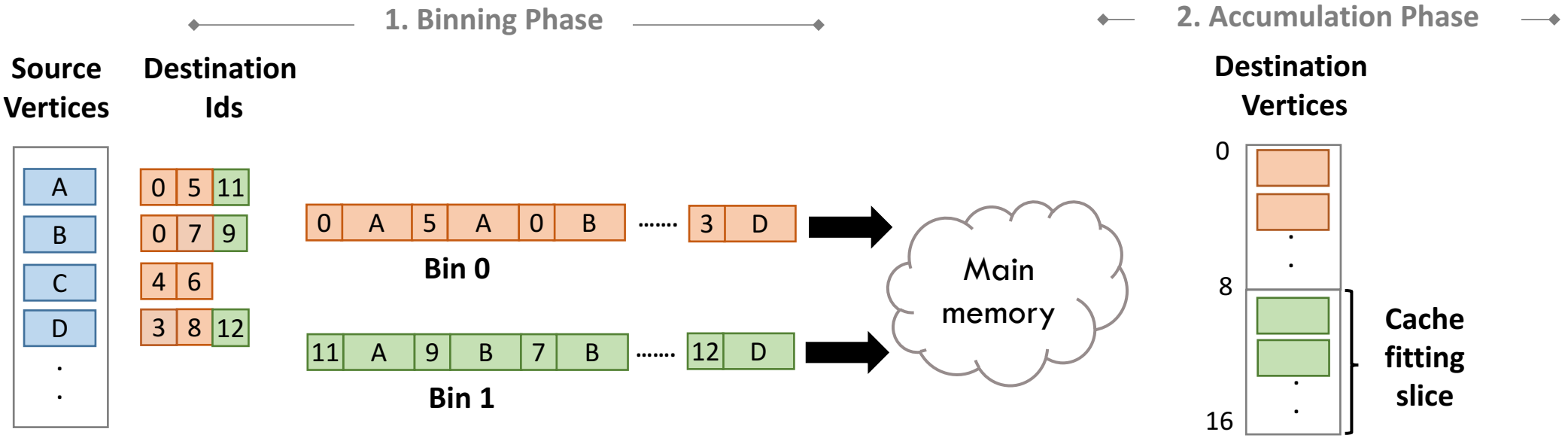

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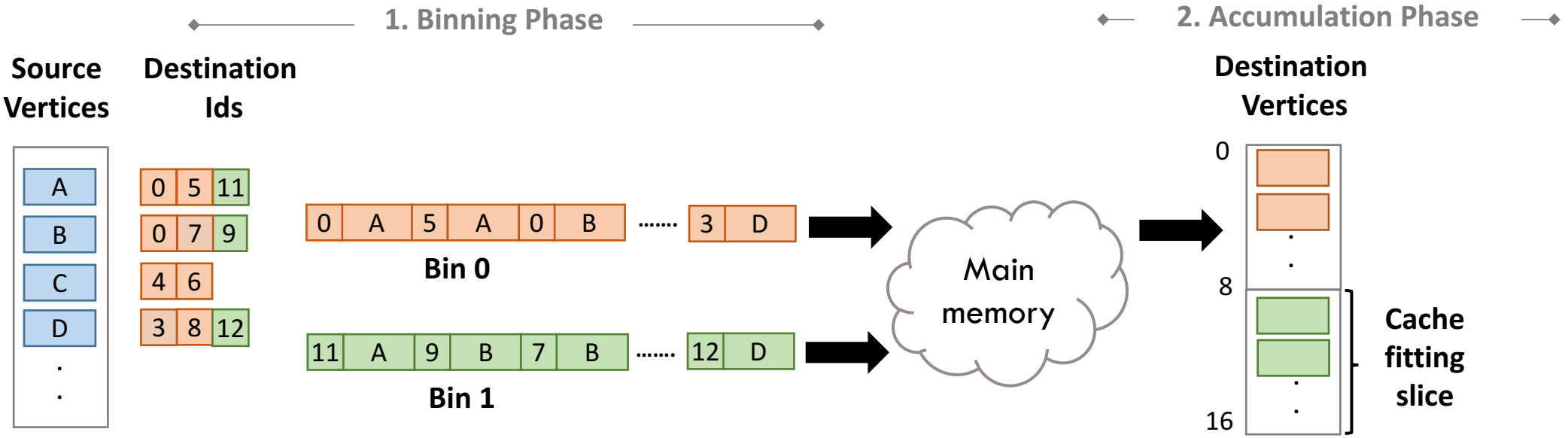

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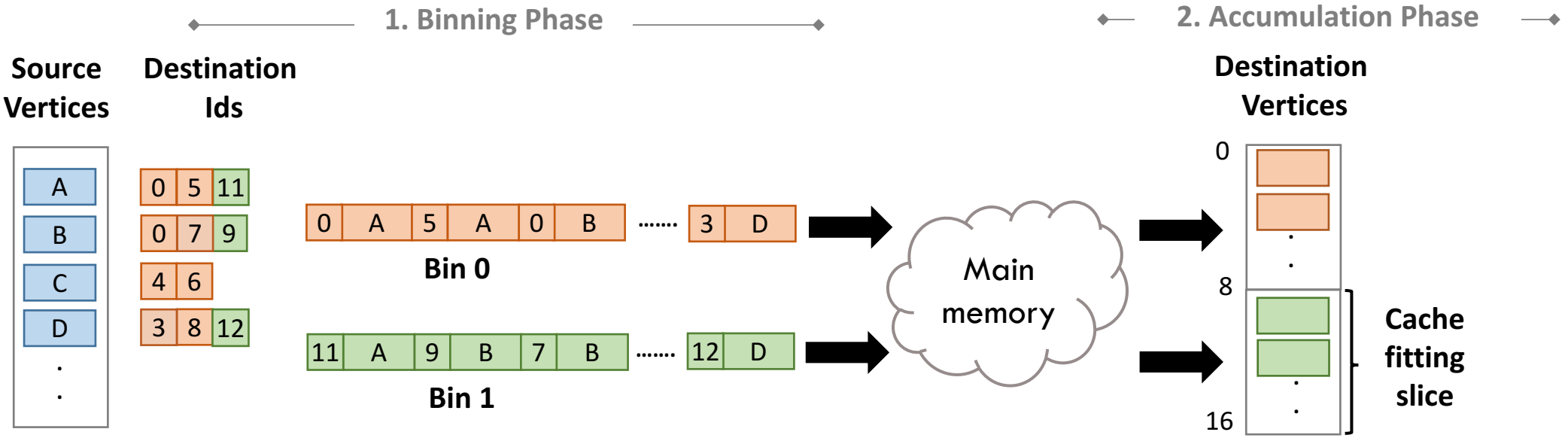

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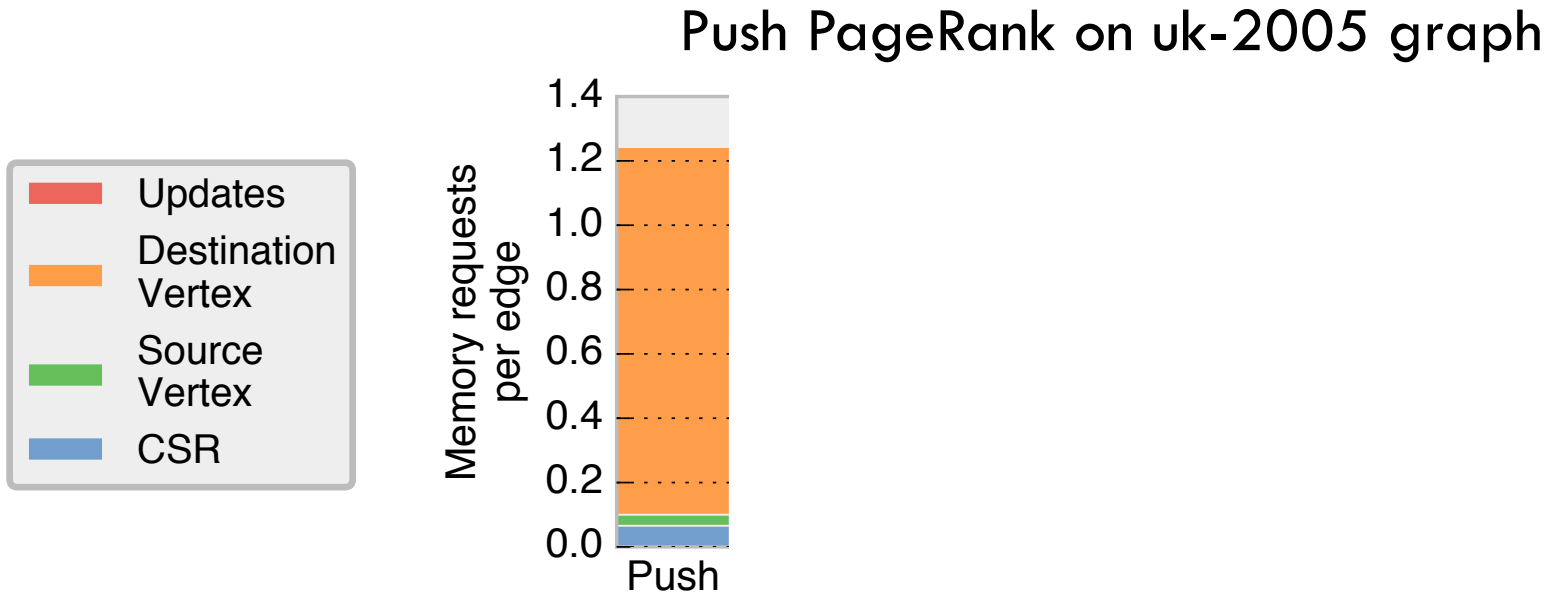

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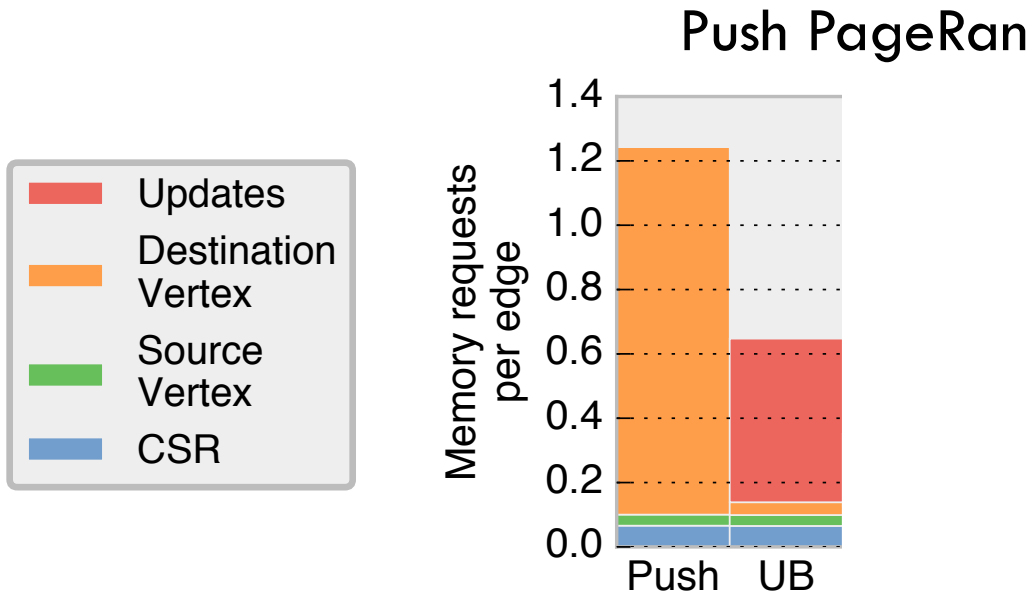

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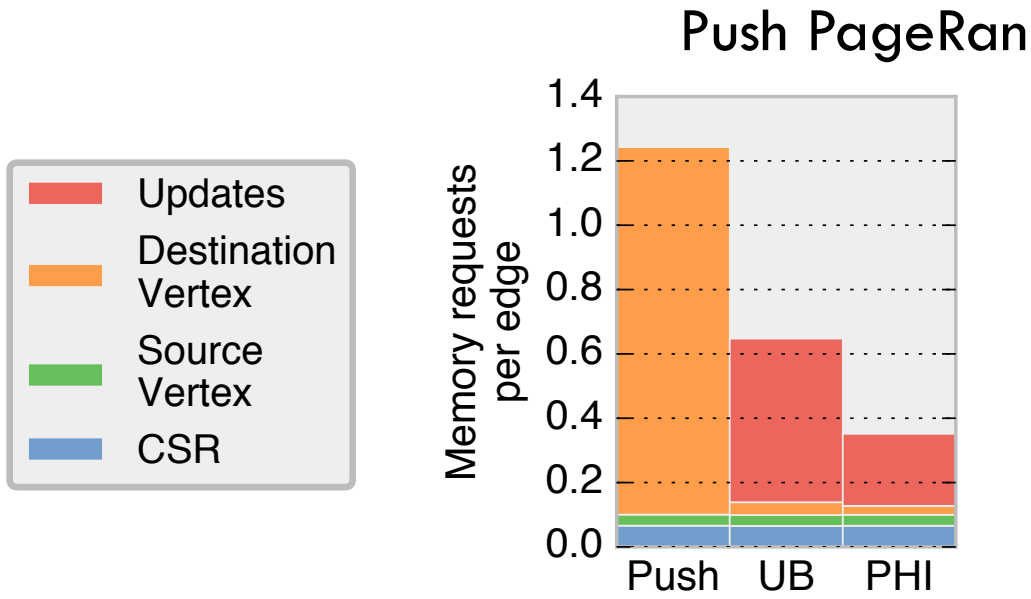

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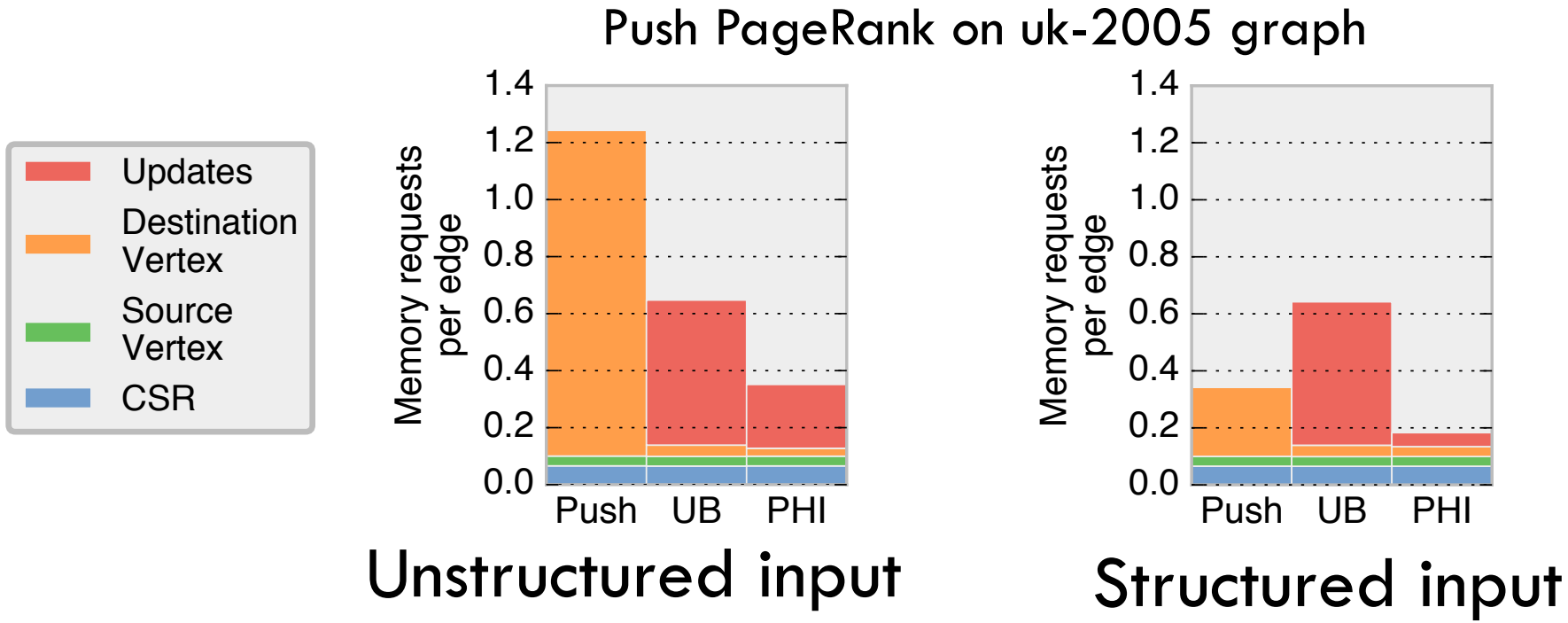

Agenda

- Background
- **PHI Design**
- Evaluation

Key techniques of PHI

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- In-cache update buffering and coalescing
  - Exploits temporal locality

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Bandwidth efficient

- Hierarchical buffering and coalescing
  - Enables update parallelism
  - Eliminates synchronization overheads

Synchronization efficient

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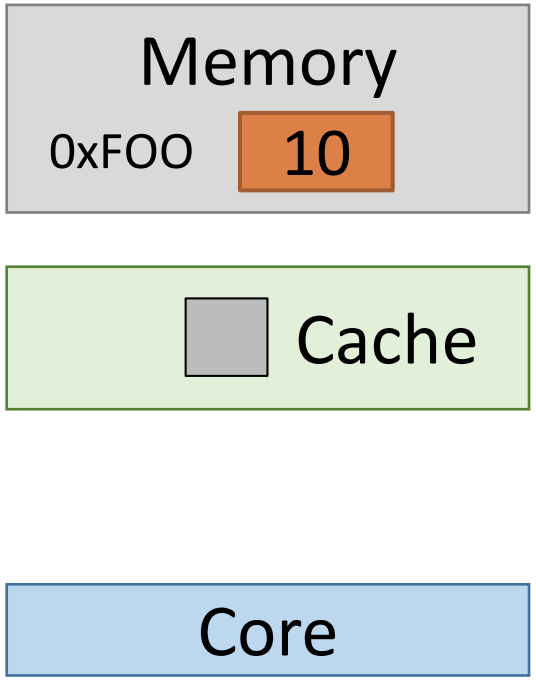

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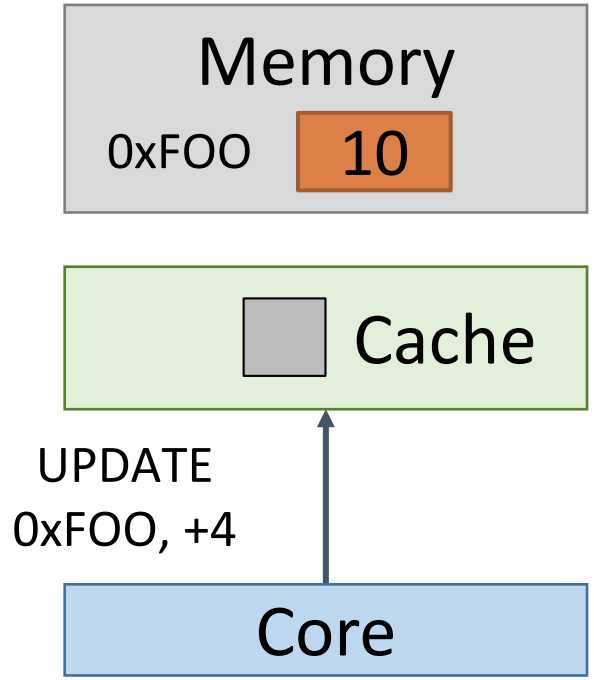

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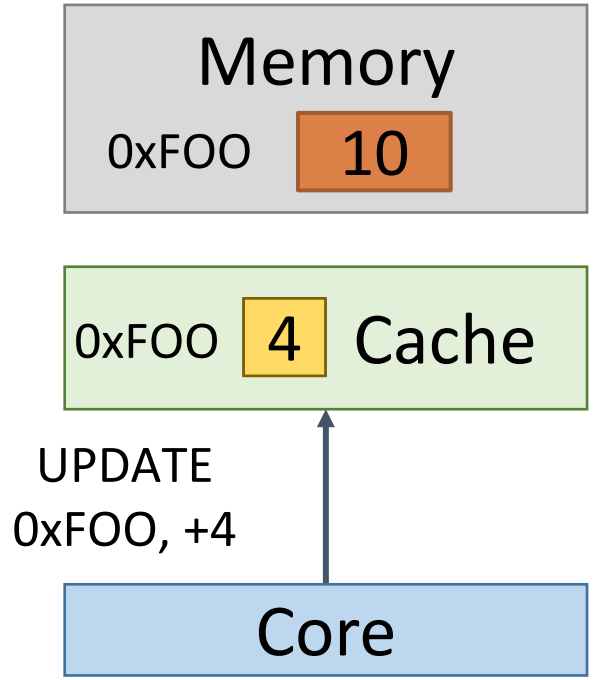

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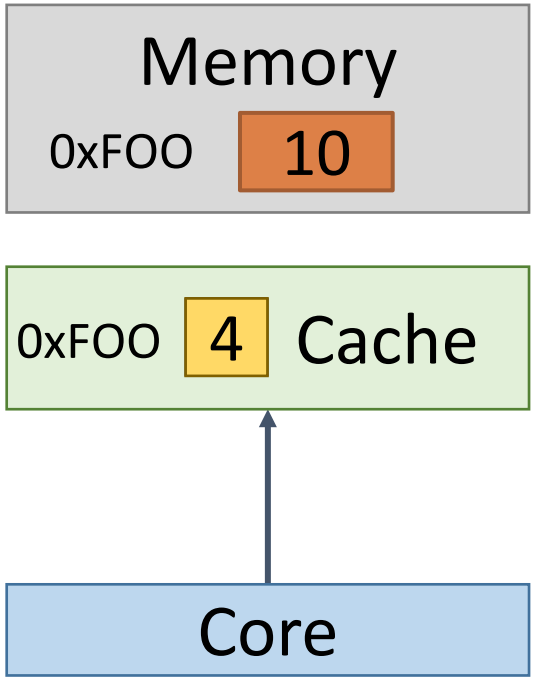

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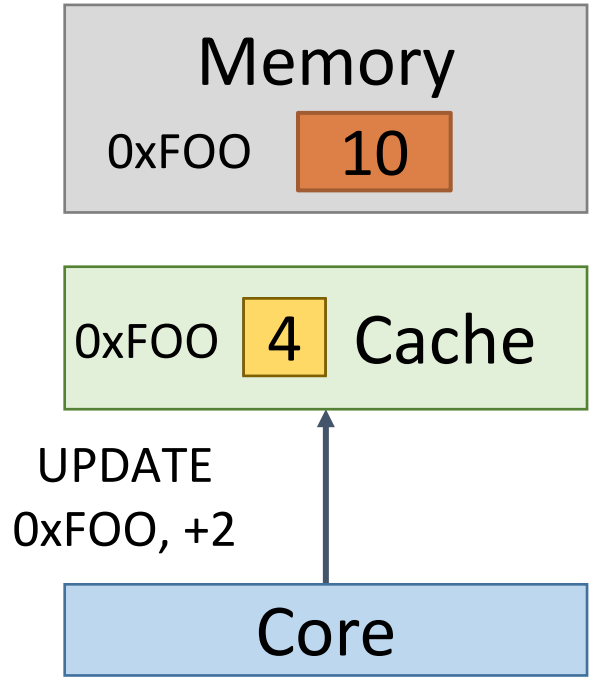

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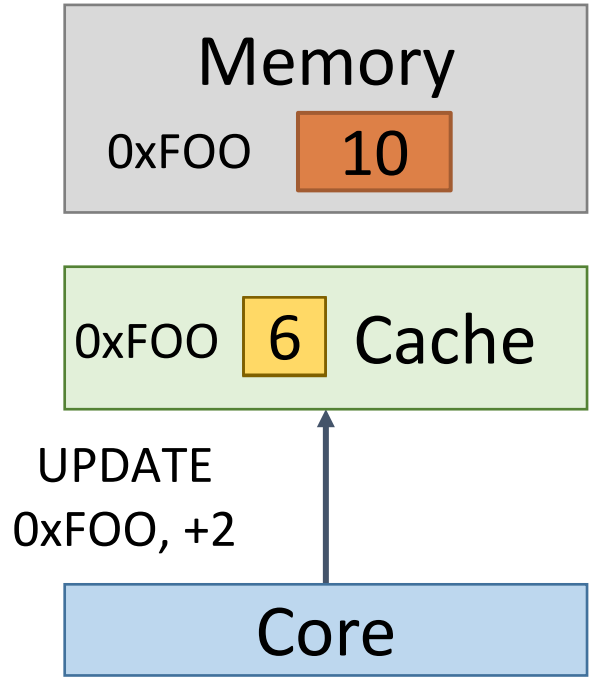

Handling cache evictions

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- Cache controller performs update batching **selectively**
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- **Key insight:** Update batching is a good tradeoff only when the evicted line has poor spatial locality

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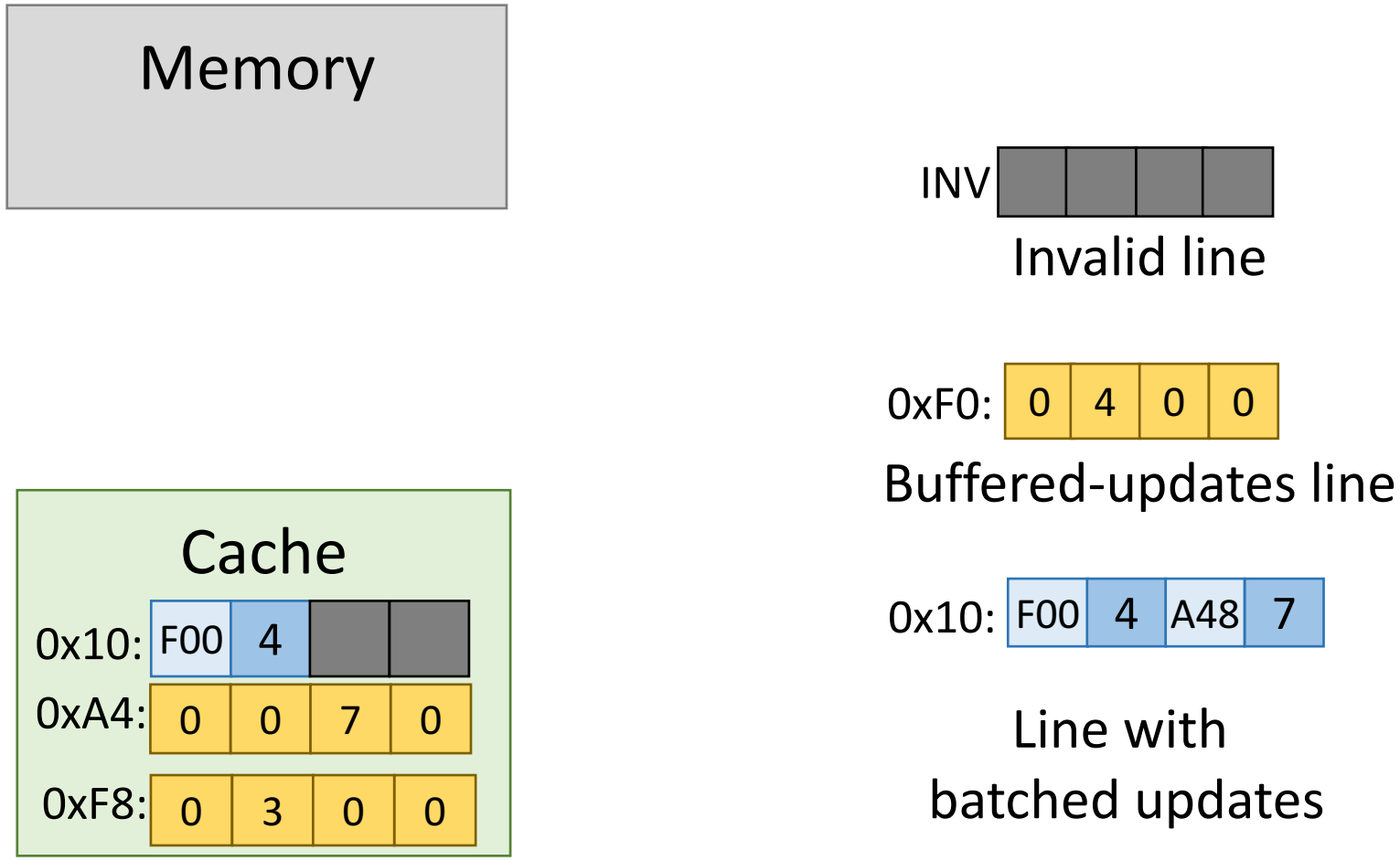

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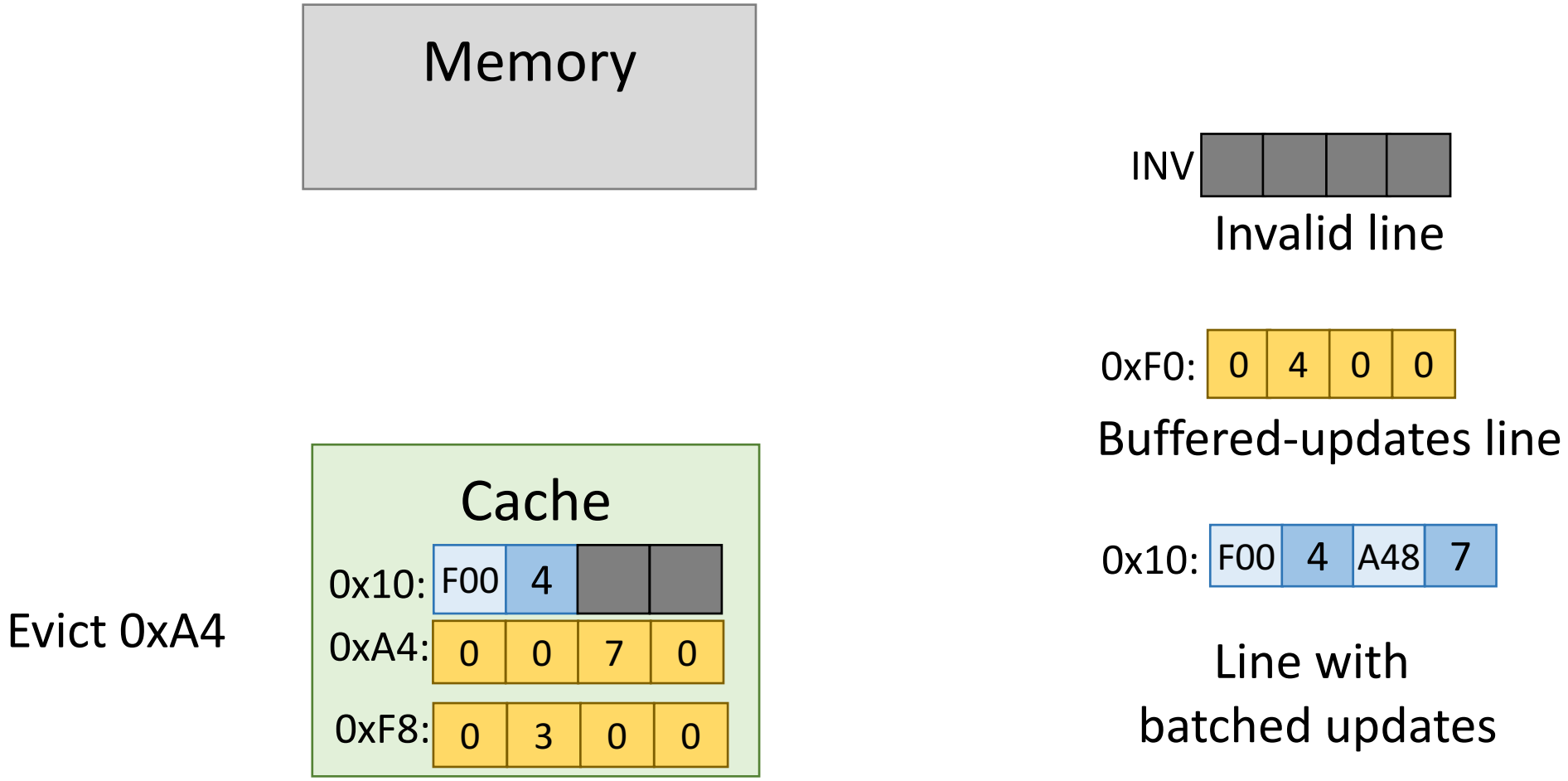

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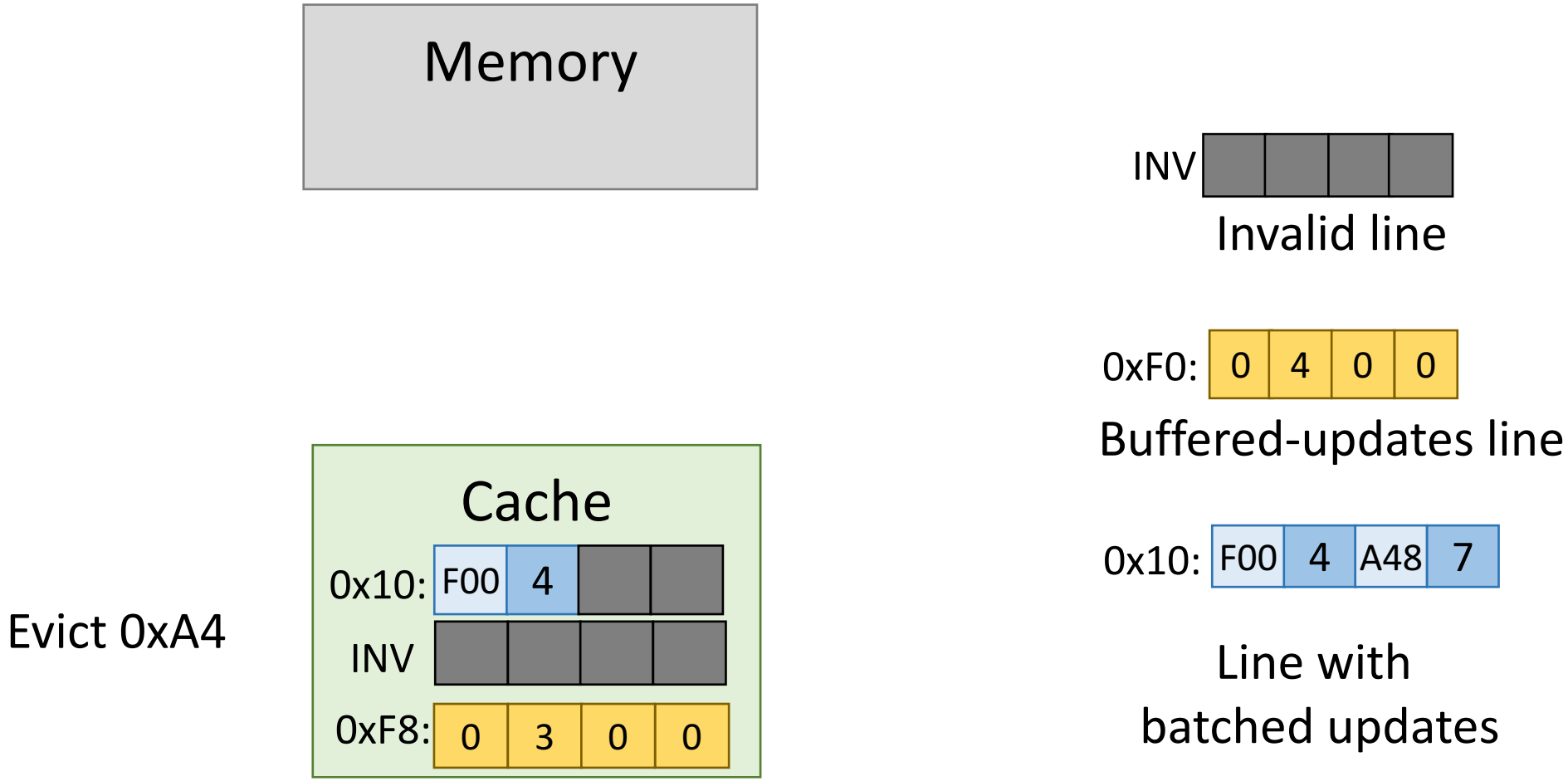

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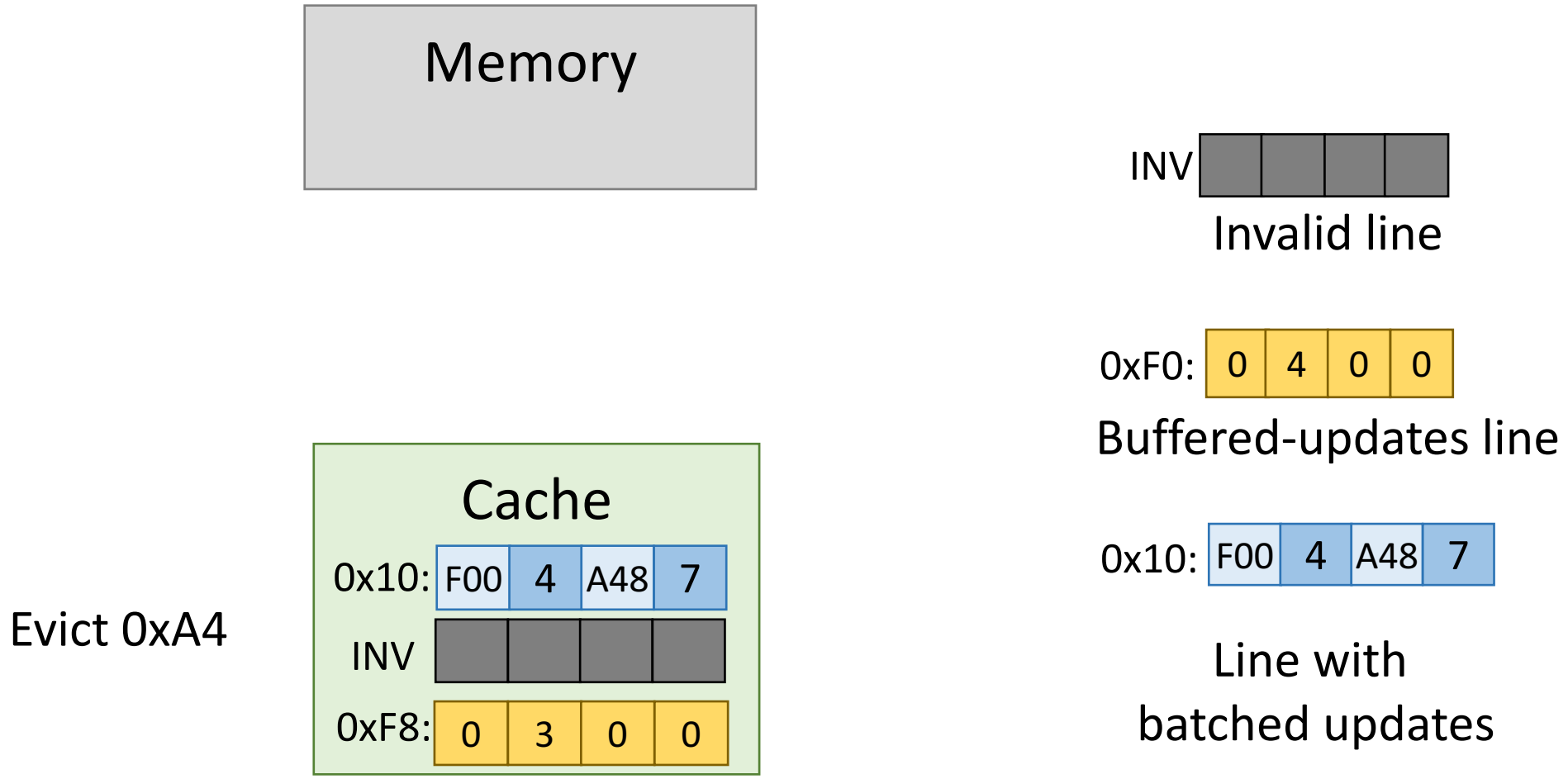

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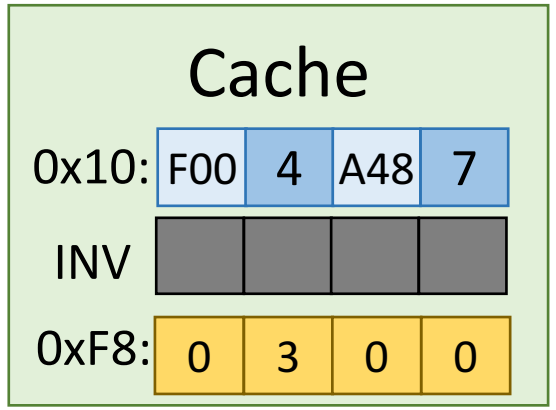

Invalid line

Buffered-updates line

Line with batched updates

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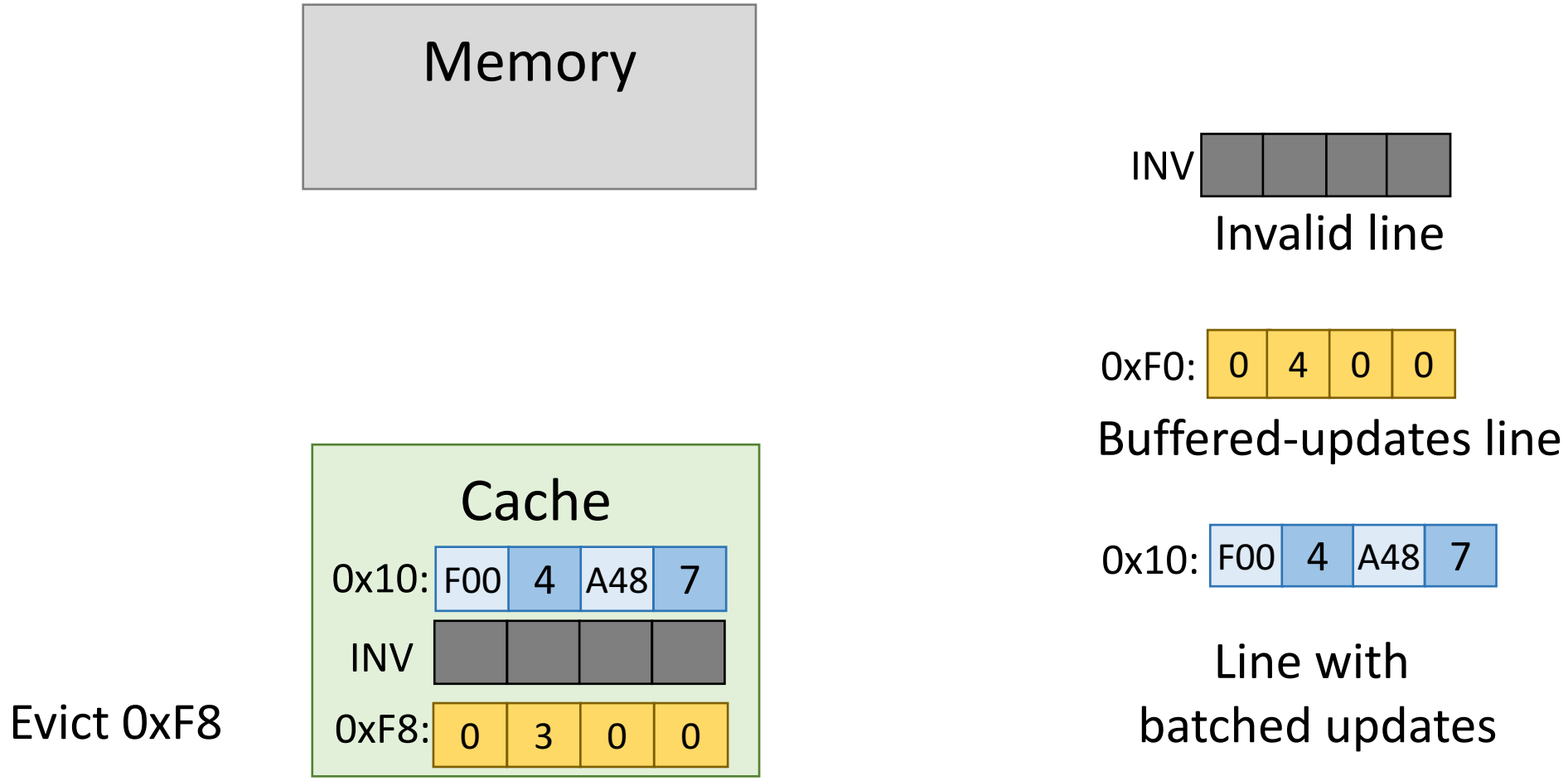

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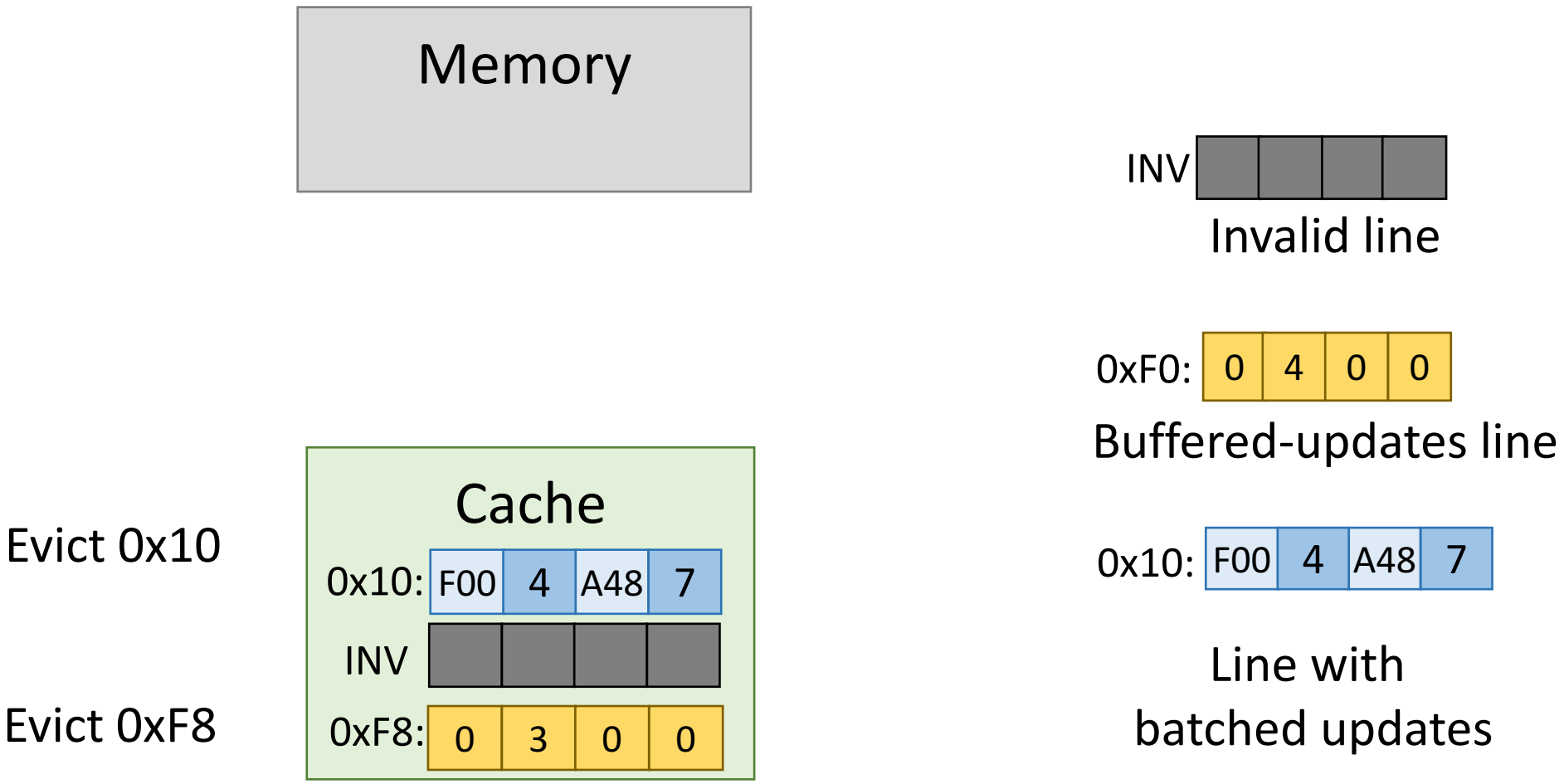

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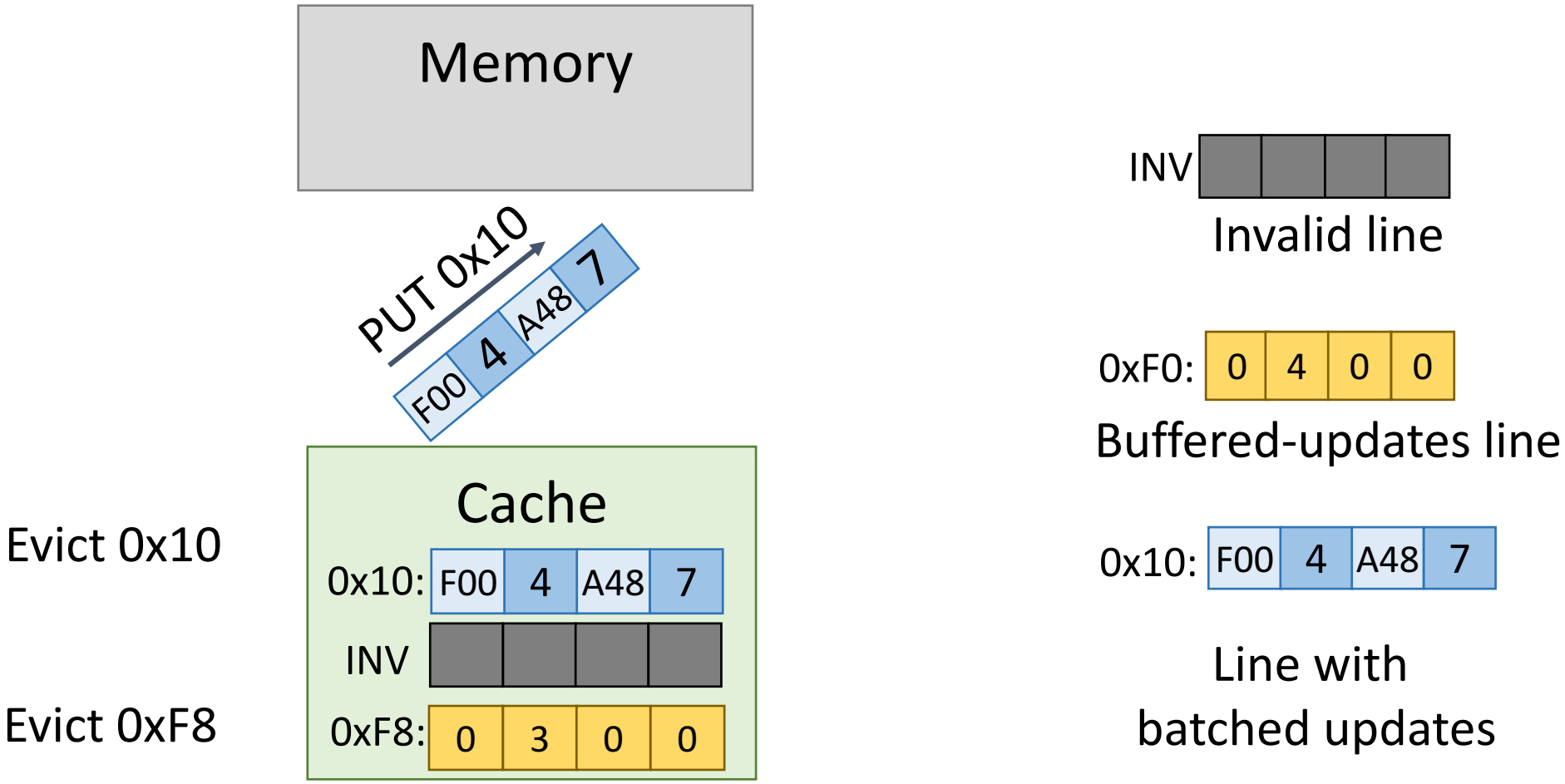

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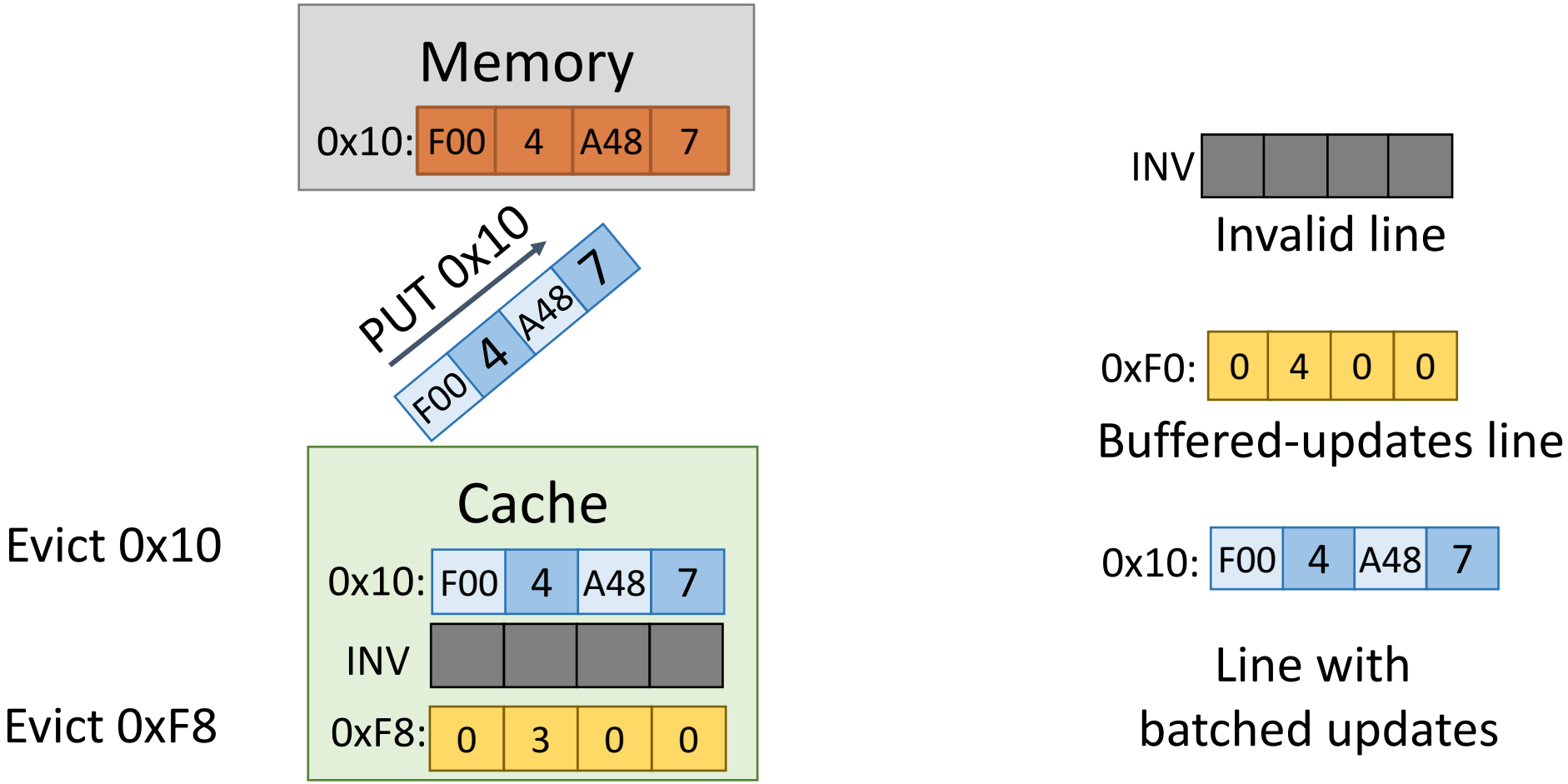

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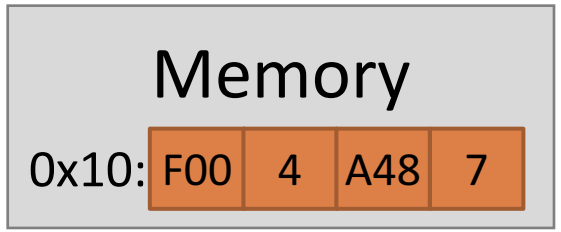

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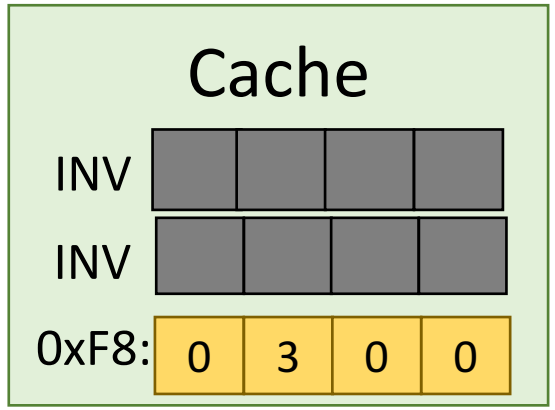

Evict 0xF8

Line with batched updates

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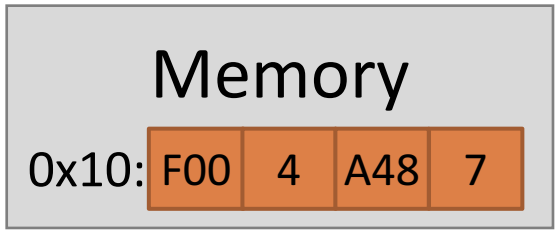

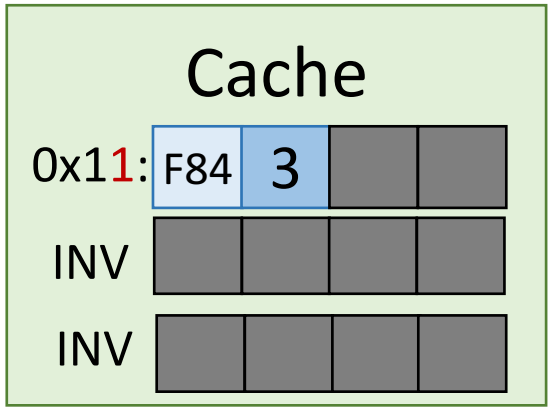

Invalid line

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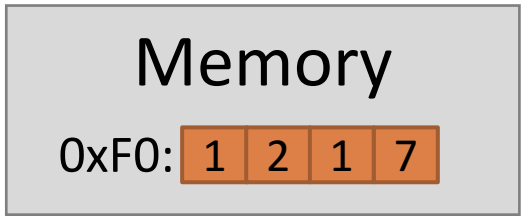

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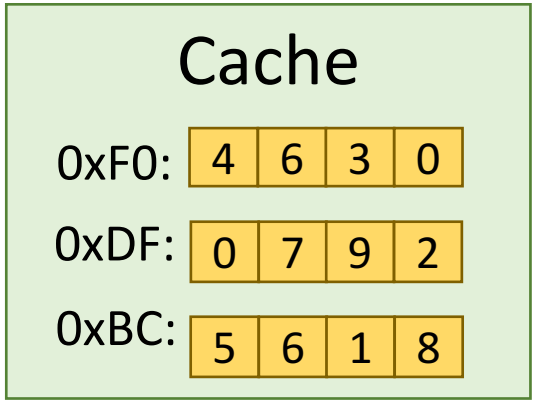

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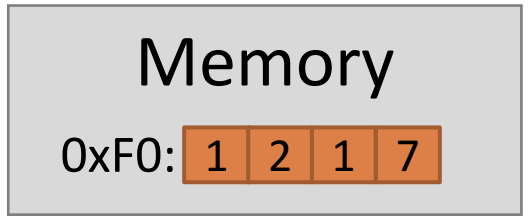

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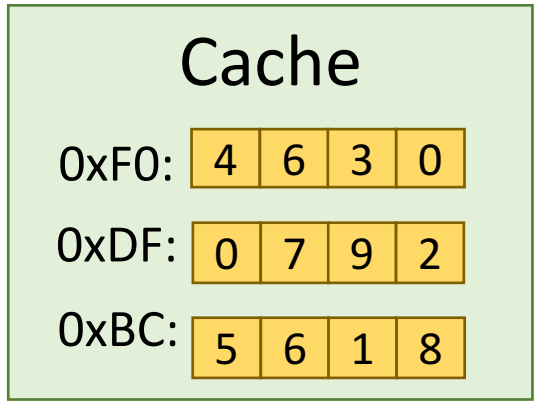

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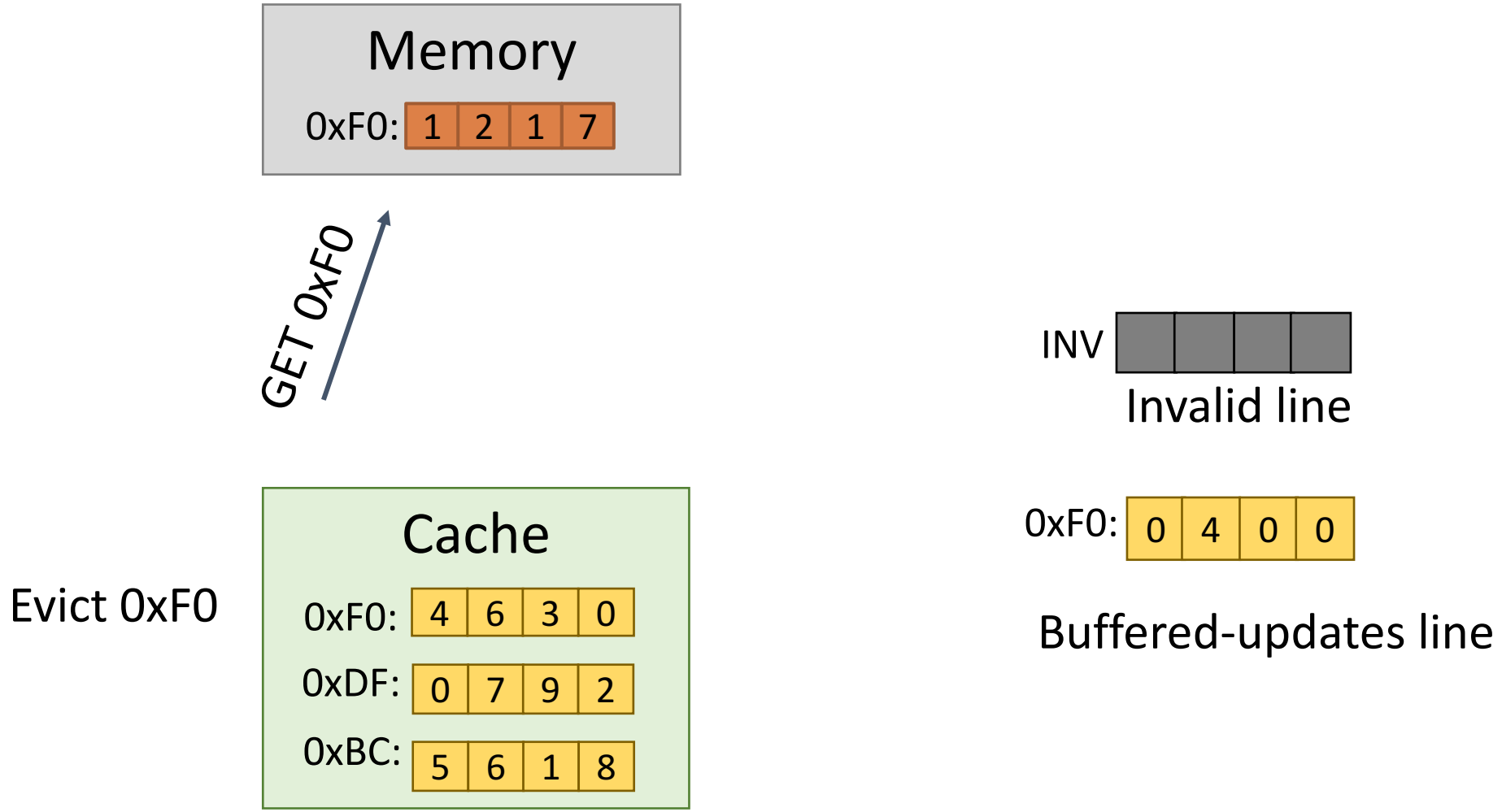

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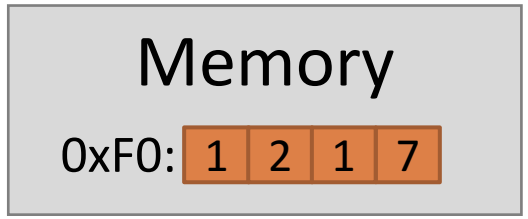

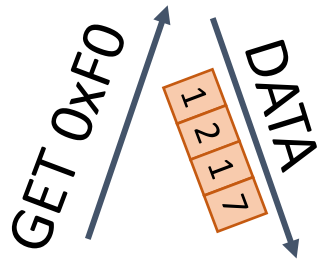

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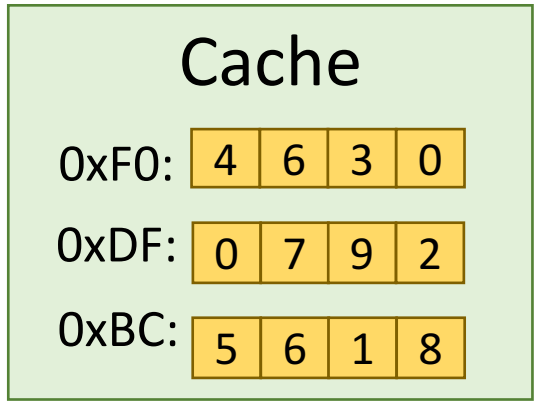

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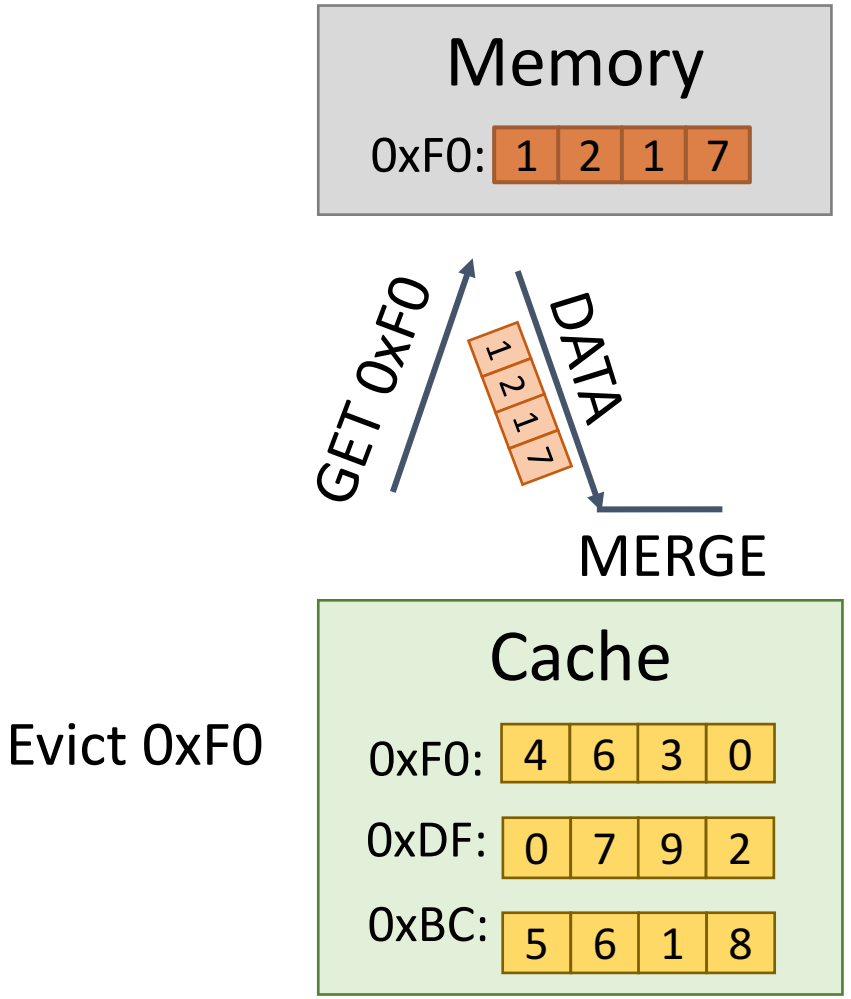

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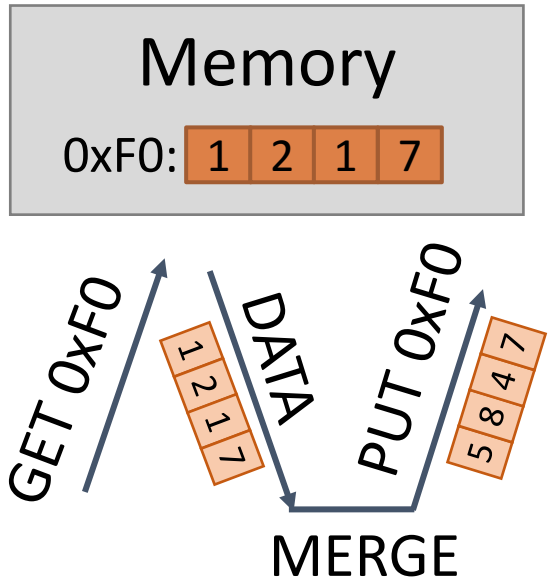

Evict 0xF0

Cache

0xF0:	4	6	3	0
0xDF:	0	7	9	2
0xBC:	5	6	1	8

Invalid line

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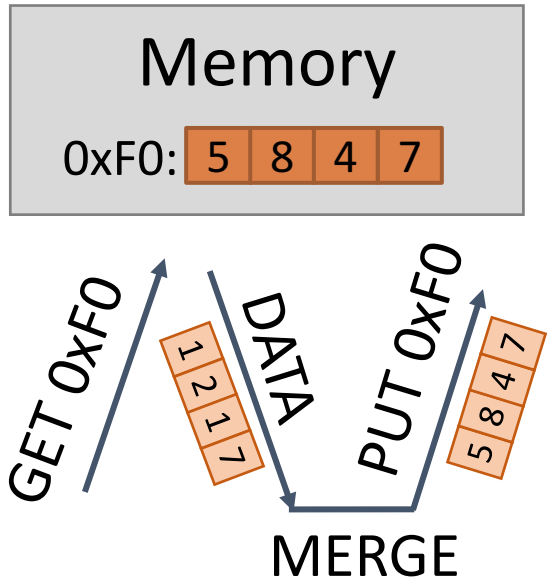

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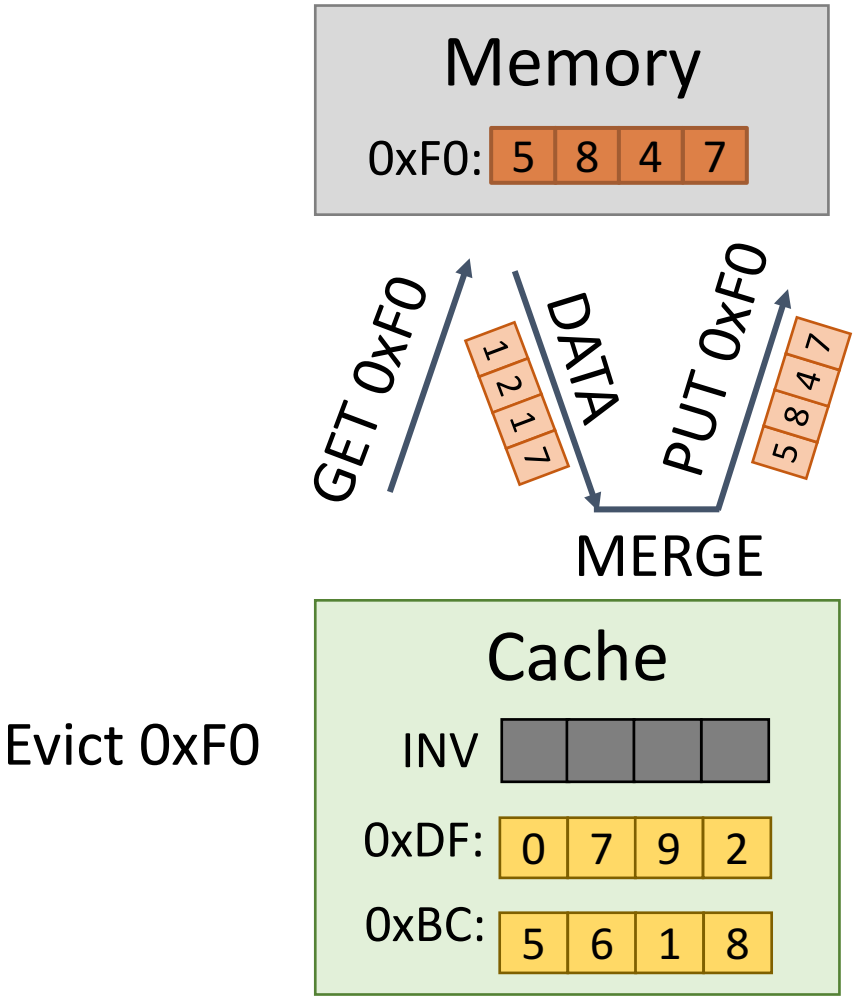

Invalid line

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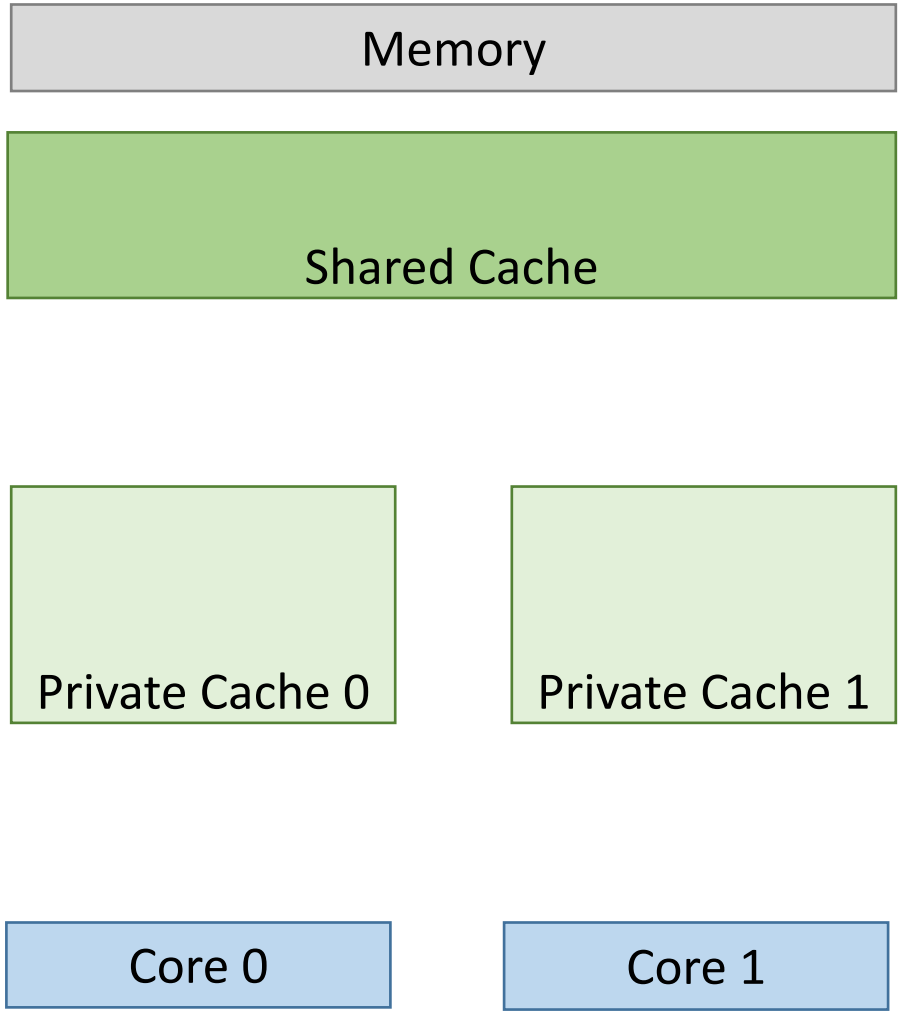

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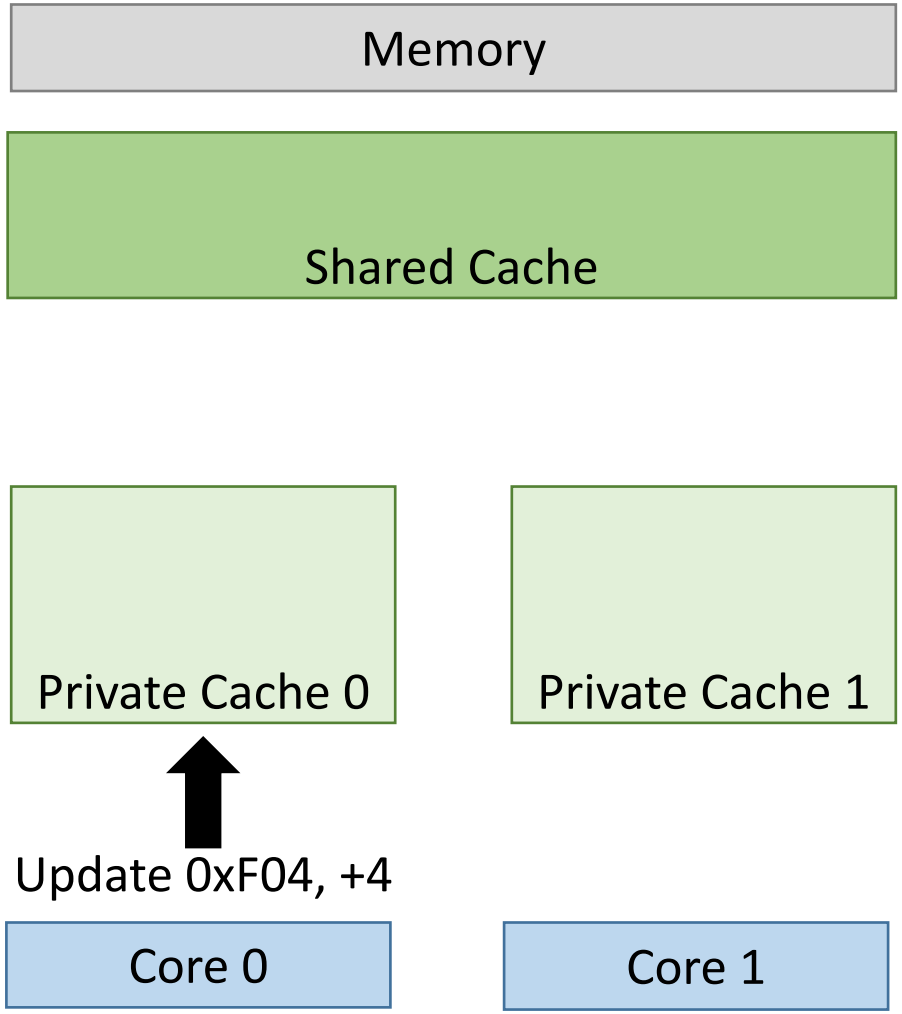

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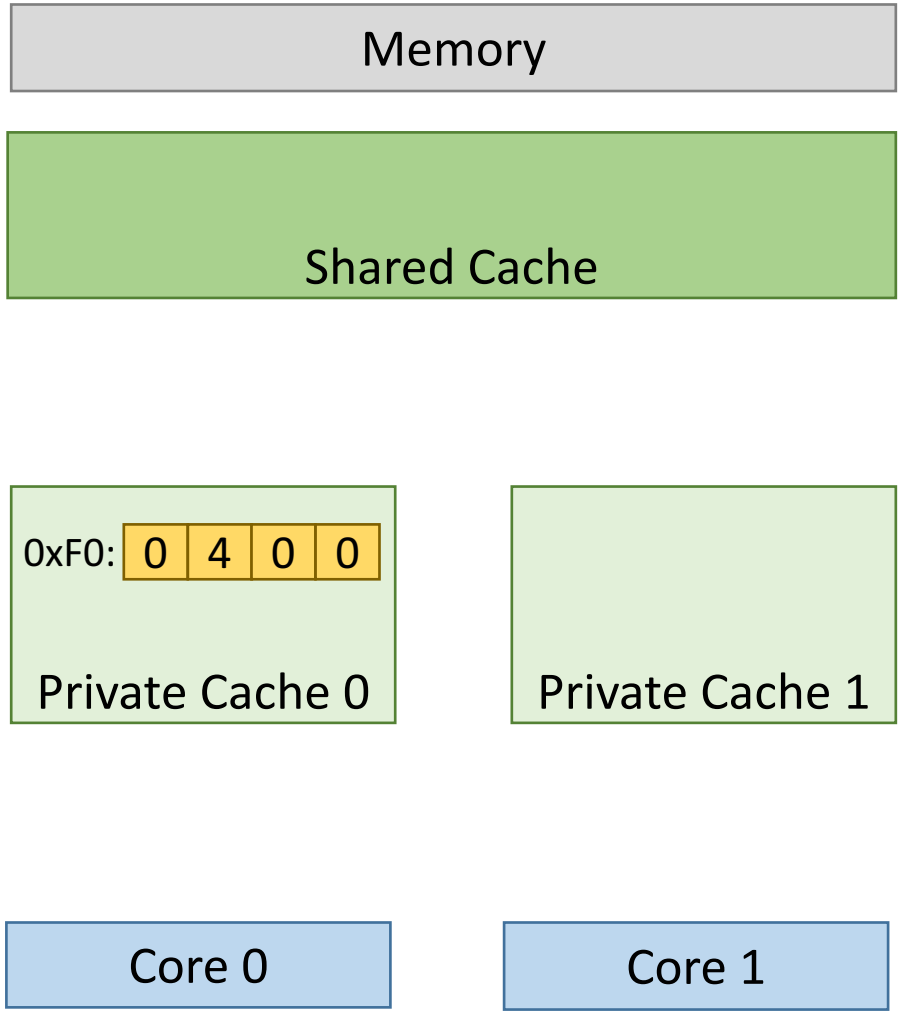

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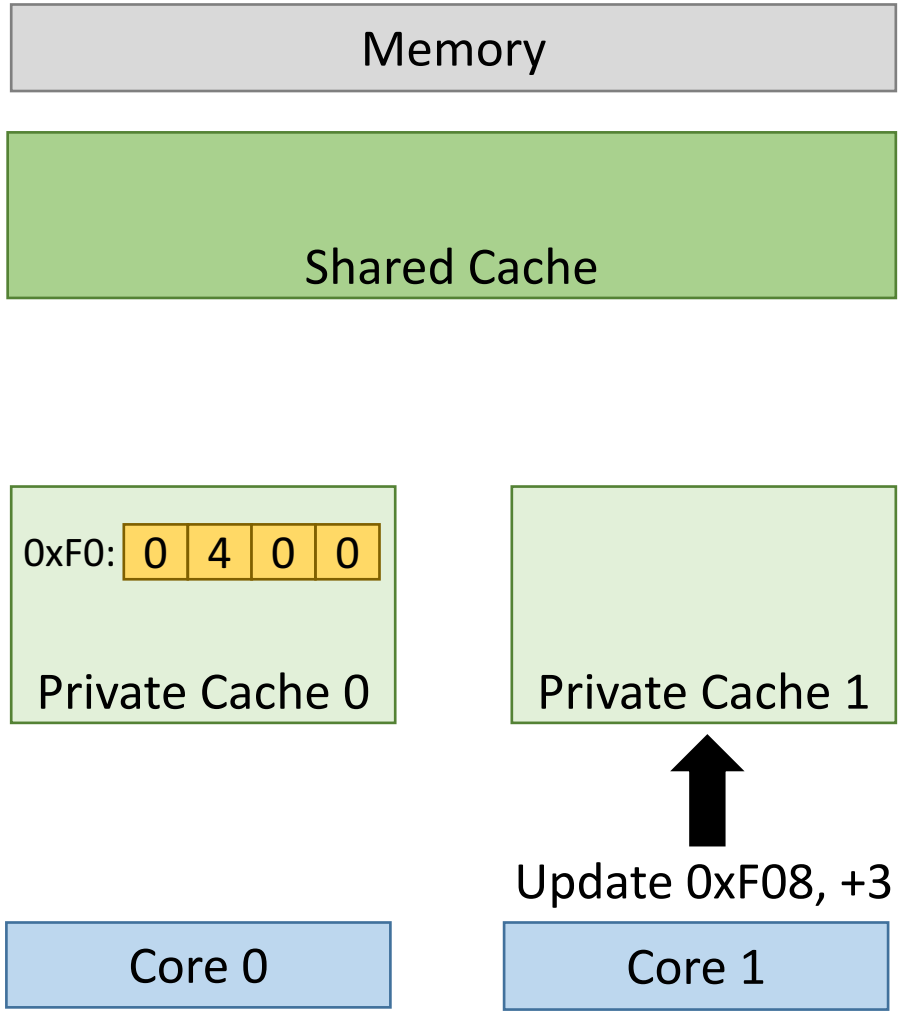

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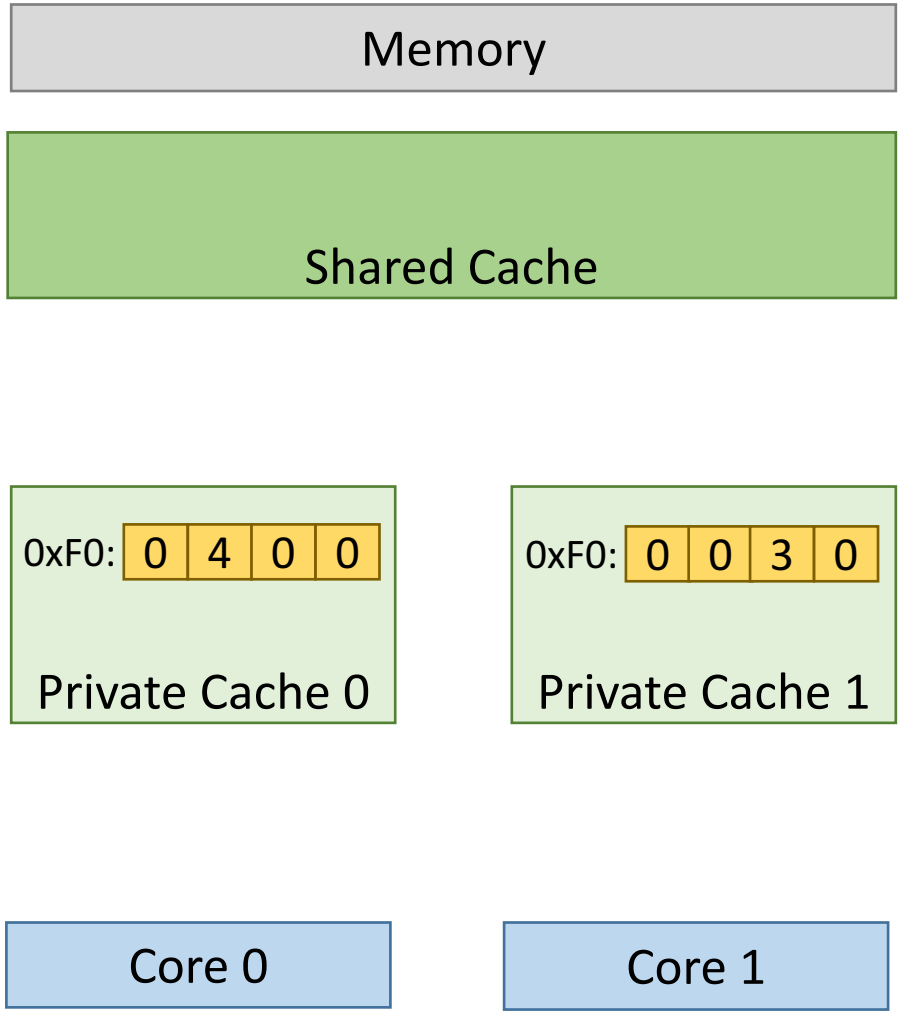

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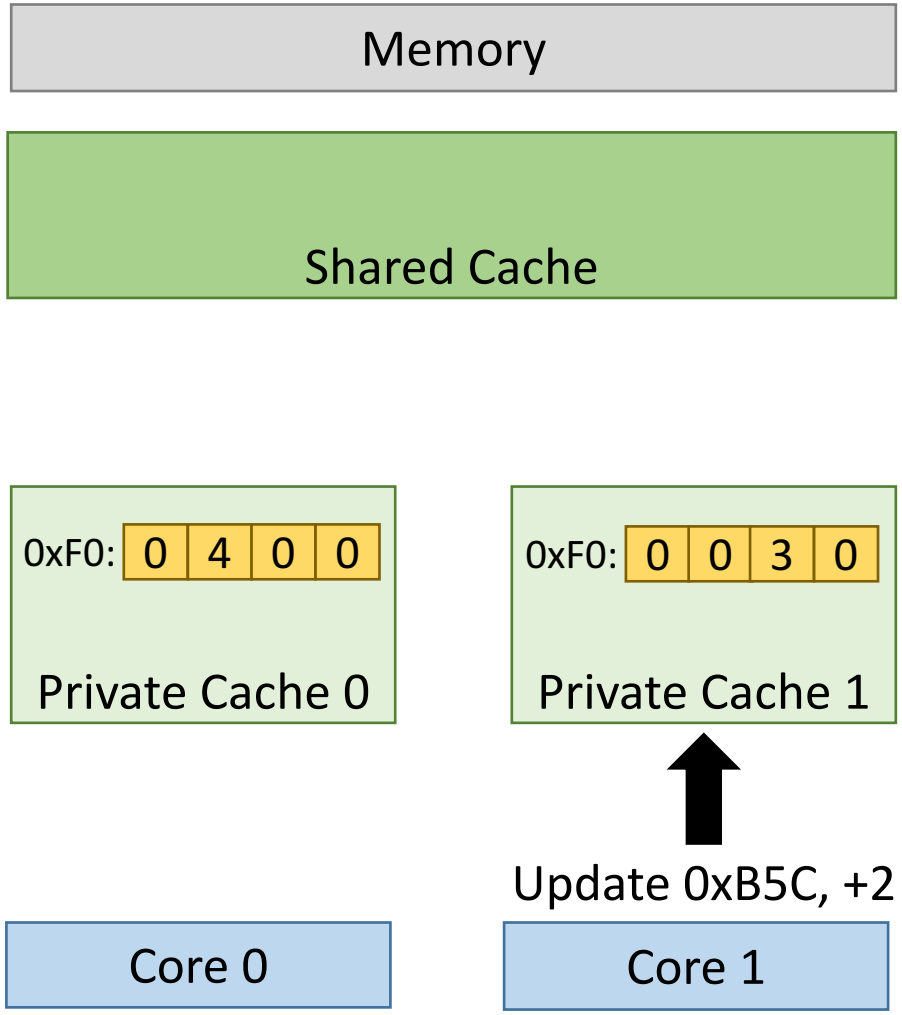

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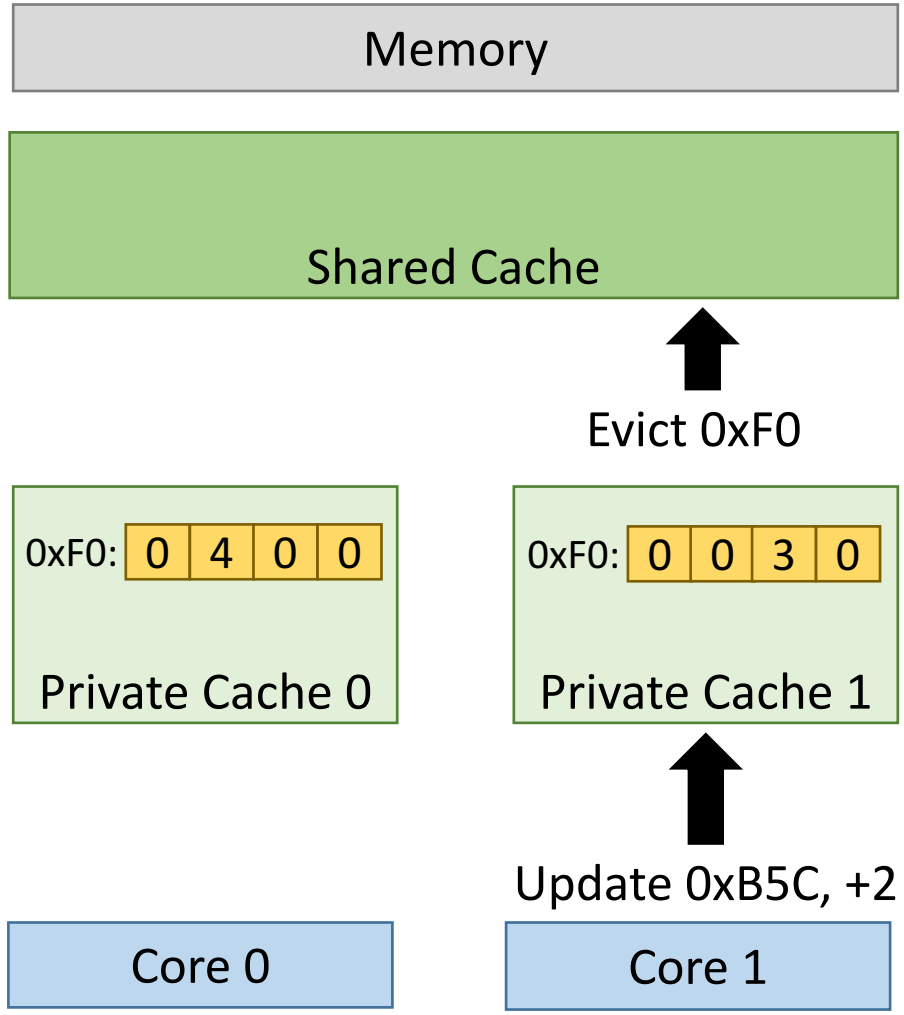

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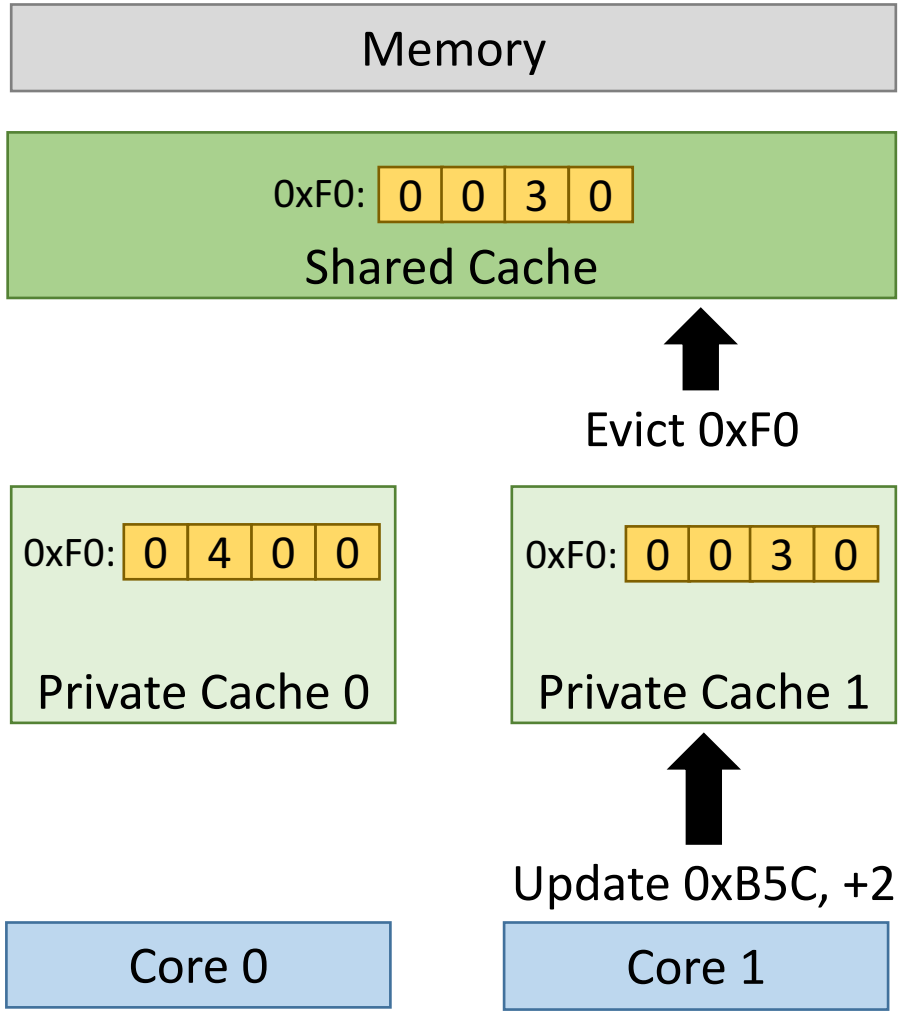

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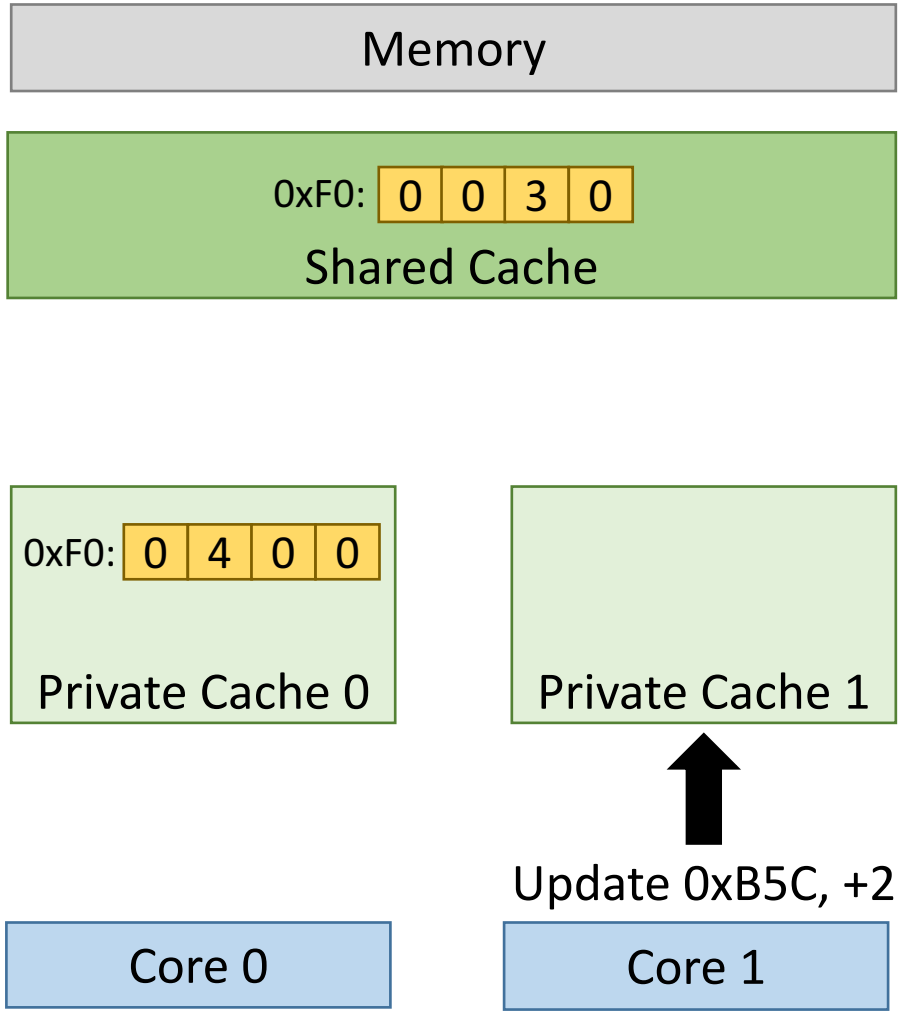

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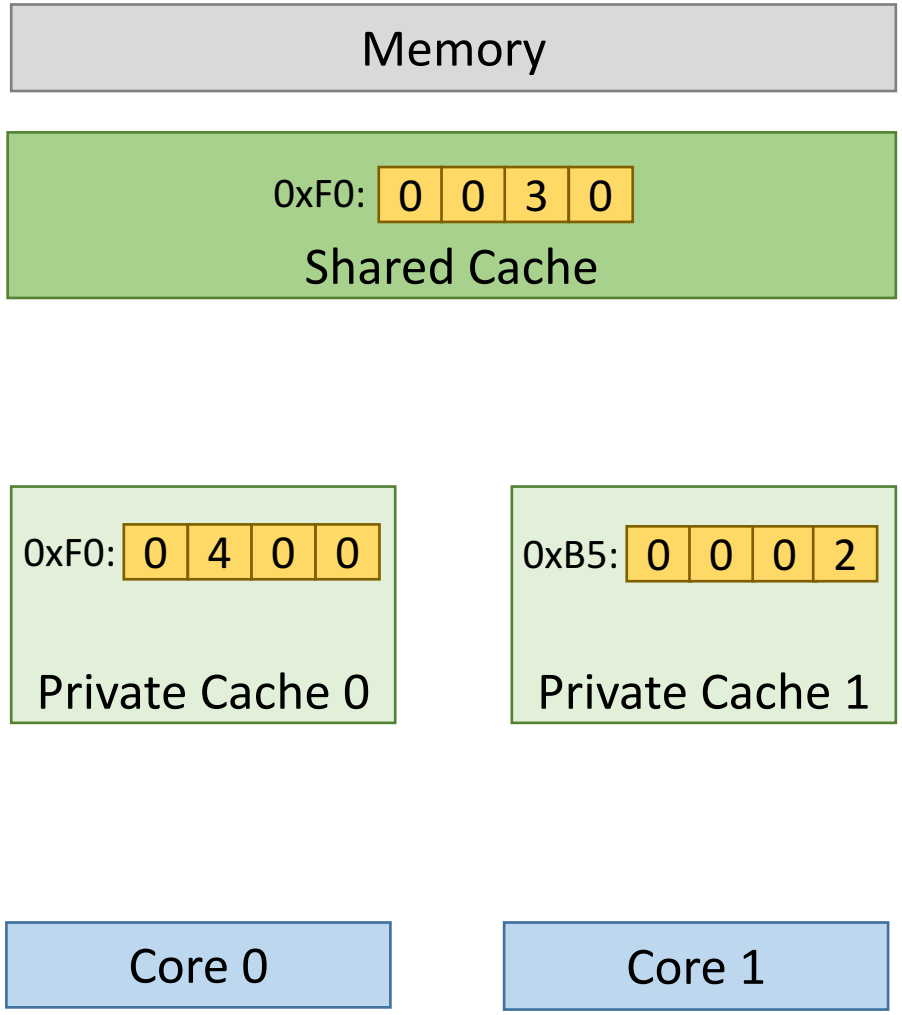

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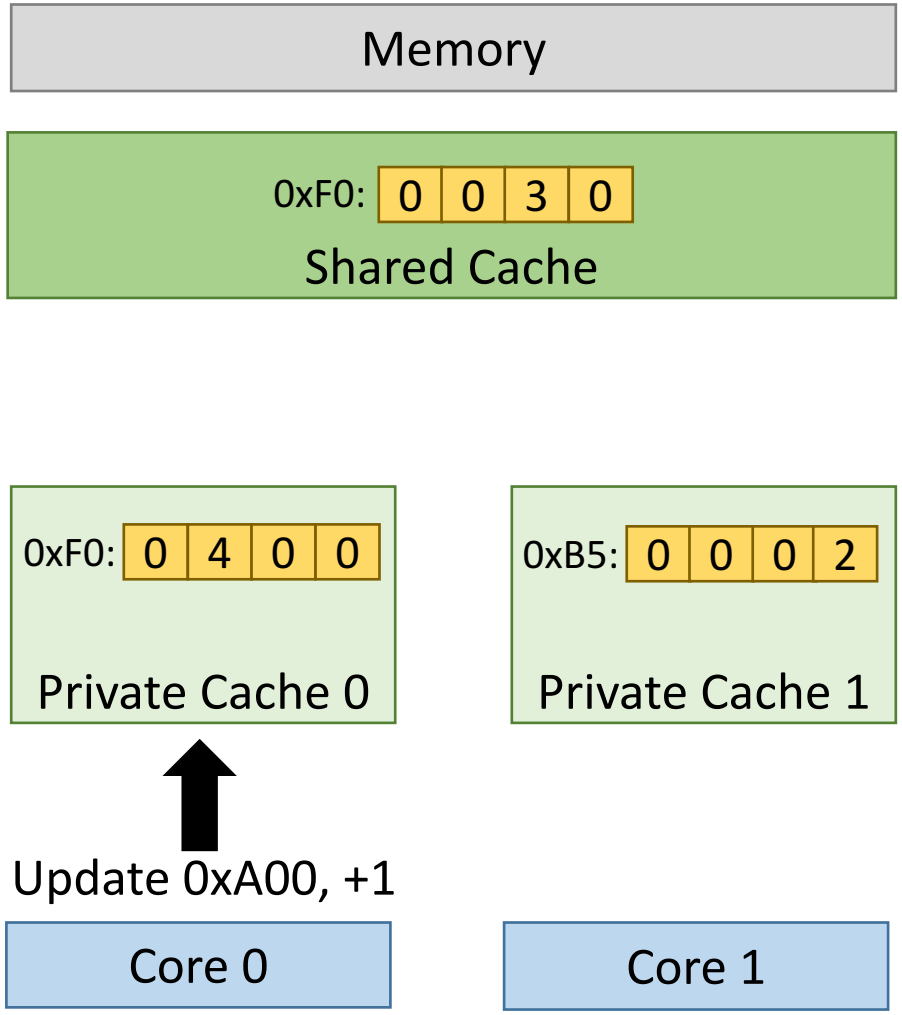

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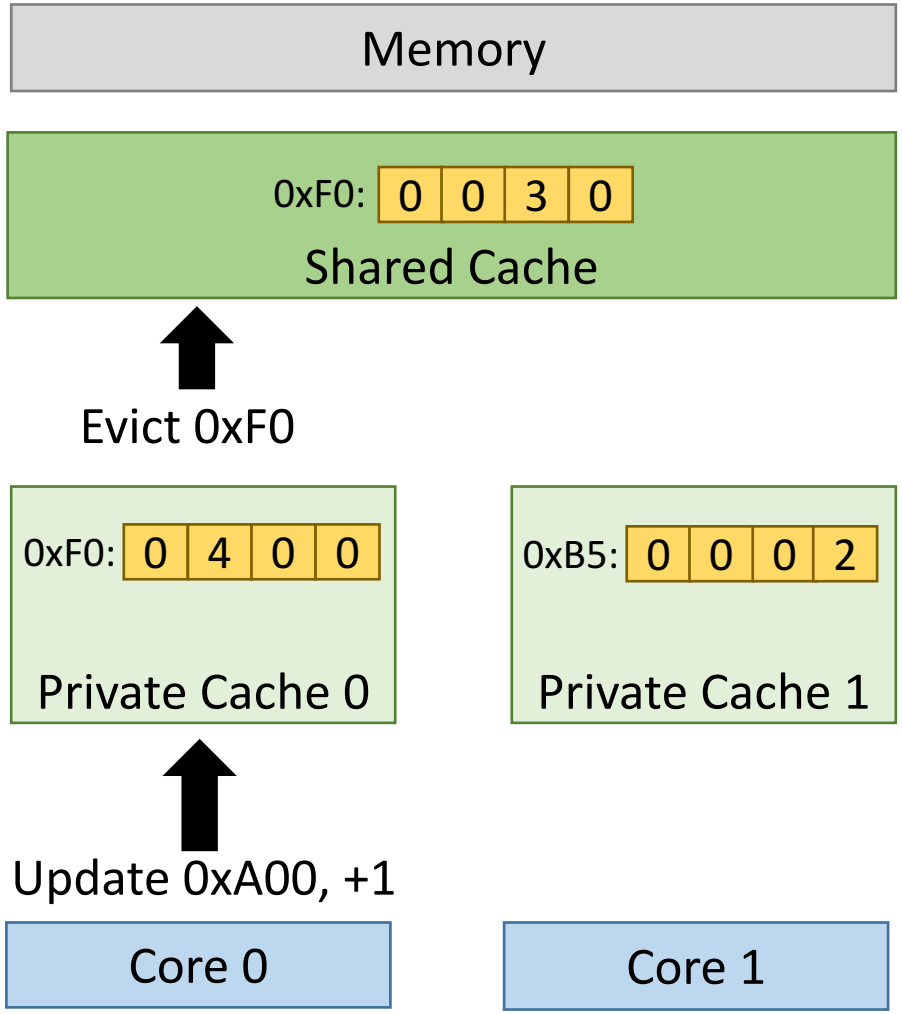

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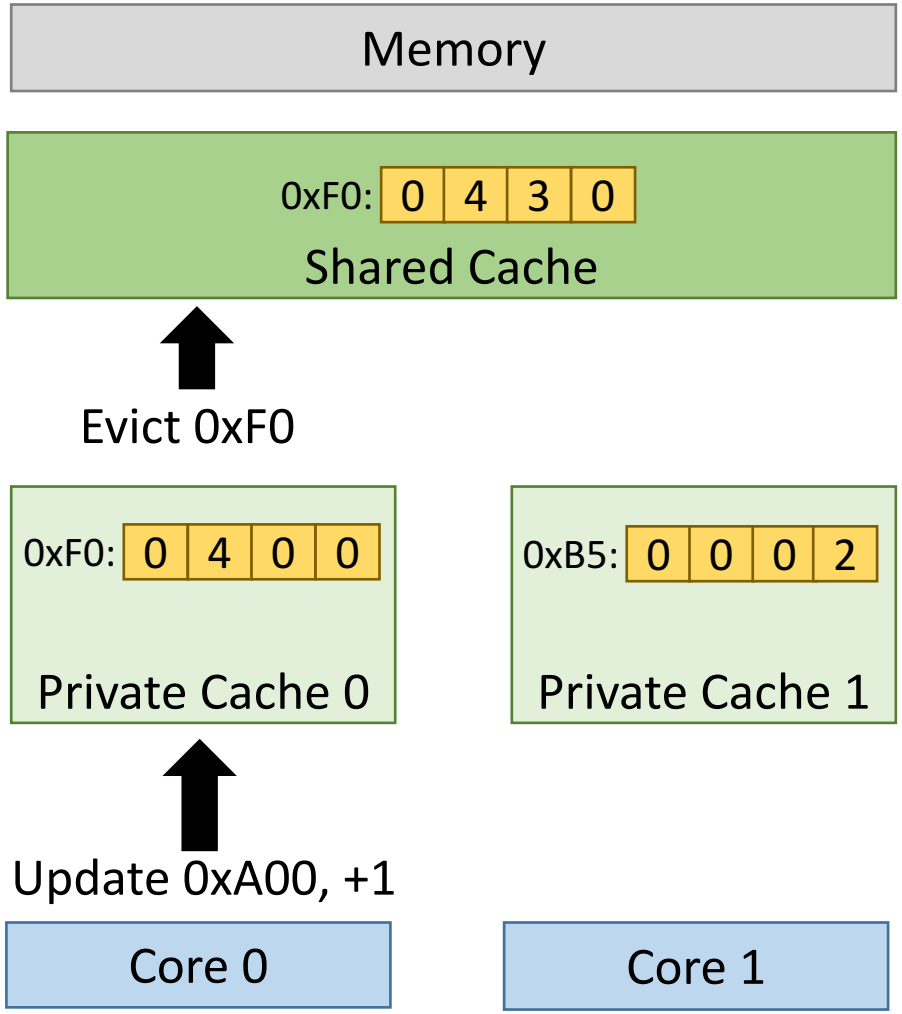

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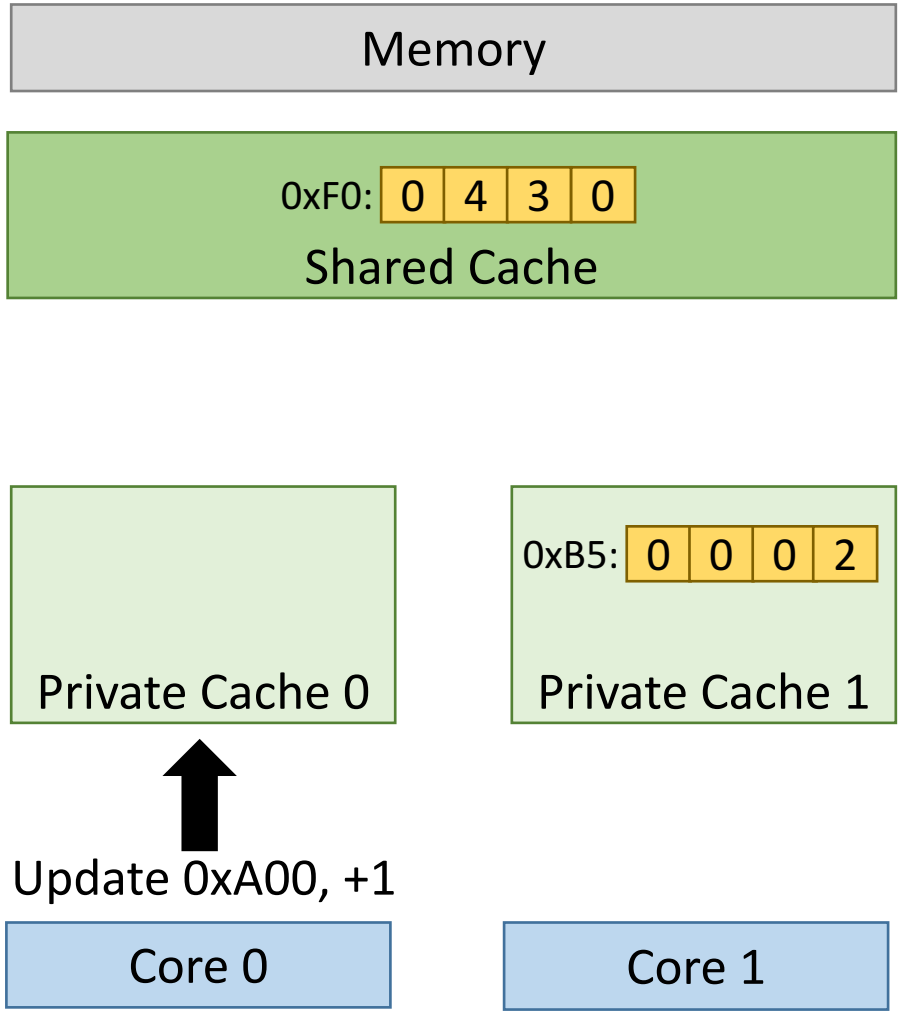

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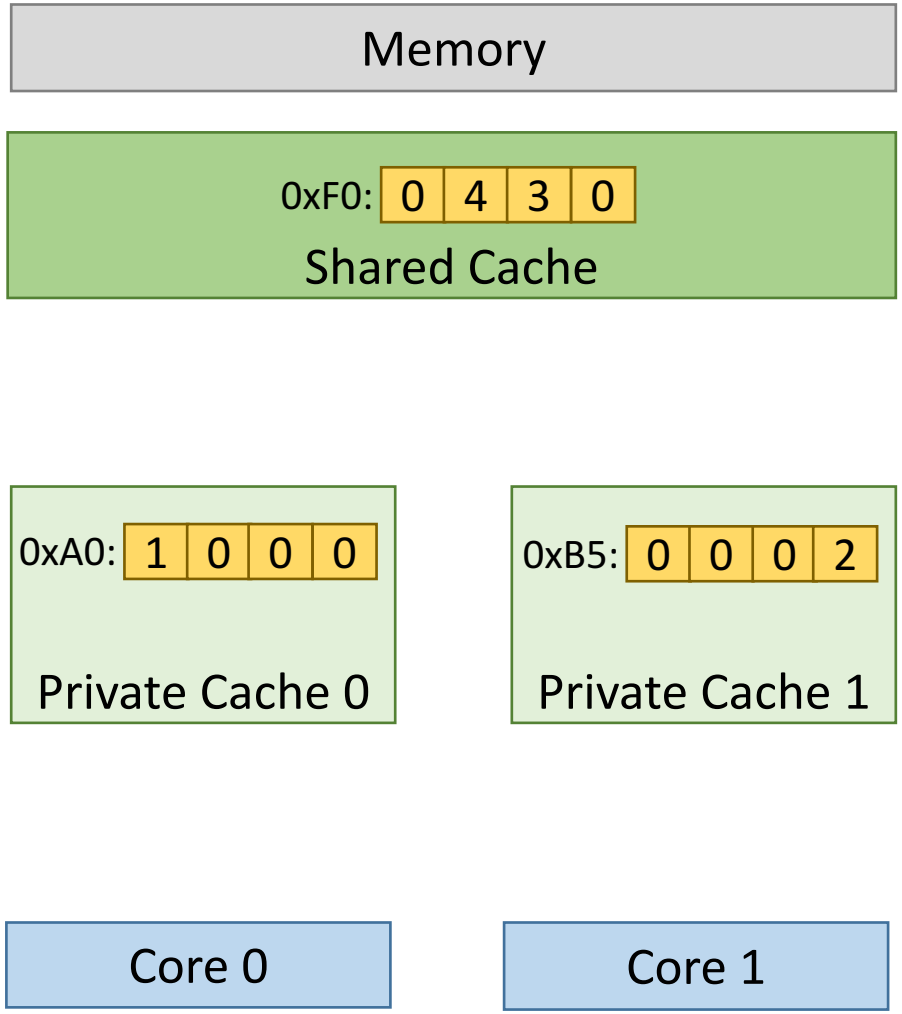

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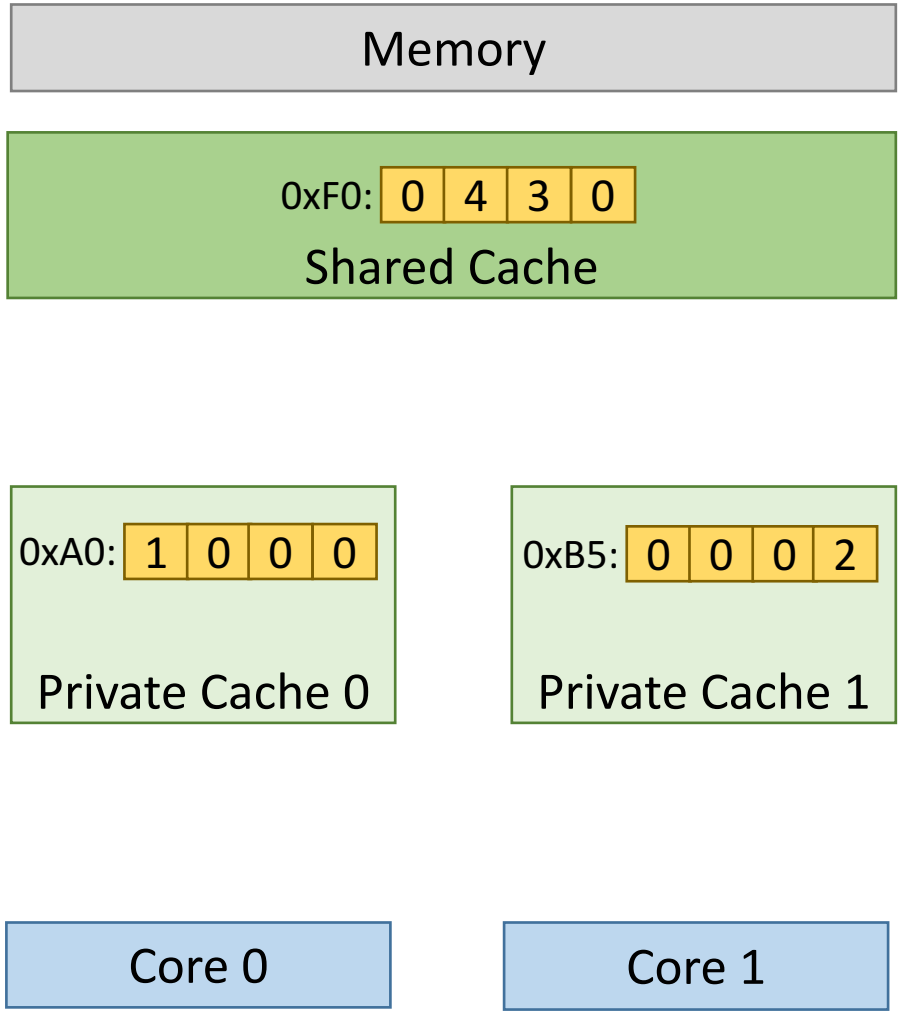
- Private caches buffer and coalesce updates locally, push them to shared cache on evictions
  - No need for a coherence protocol
- Private caches do not perform update batching
  - Simply evict buffered-update lines to shared cache



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- Per-line buffered updates bit
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- Per-line buffered updates bit
  - 0.17% additional storage with 64-byte lines
- Reduction unit for each cache bank
  - Supports 64-bit floating-point and integer additions, logical operations
  - 0.06% of chip area in a 16-core system (0.09mm^2 in 45 nm)

Agenda

- Background
- PHI Design
- **Evaluation**

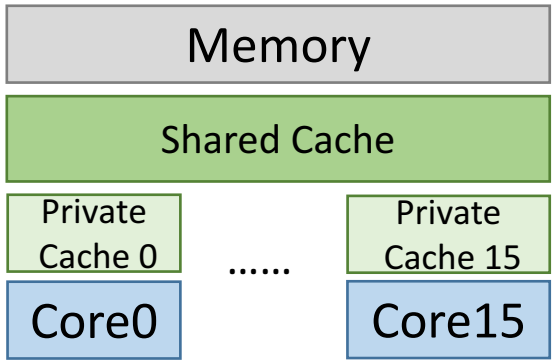
Evaluation methodology

Evaluation methodology

- Event-driven simulation using ZSim

Evaluation methodology

- Event-driven simulation using ZSim
- 16-core processor
  - Haswell-like OOO cores
  - 32 MB L3 cache
  - 4 memory controllers



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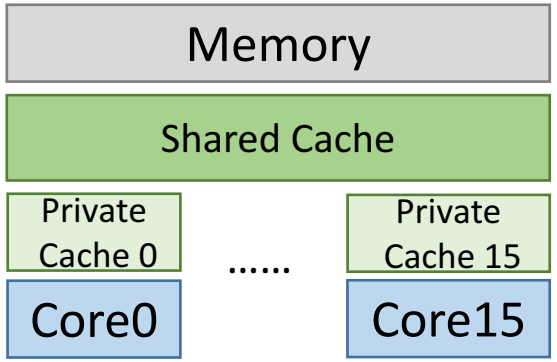

- Graph applications
  - PageRank, PageRank Delta, Connected Components, Radii Estimation
- Degree Counting (No Pull)
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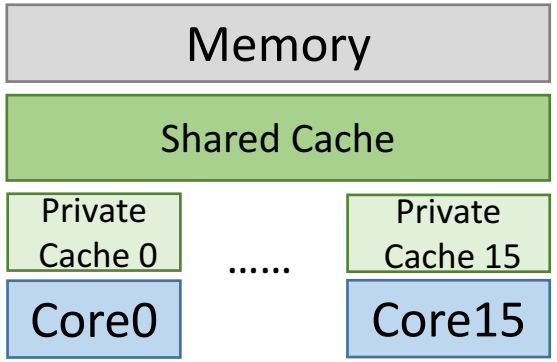

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- Large real world inputs
  - Up to 100 million vertices
  - Up to 1 billion edges

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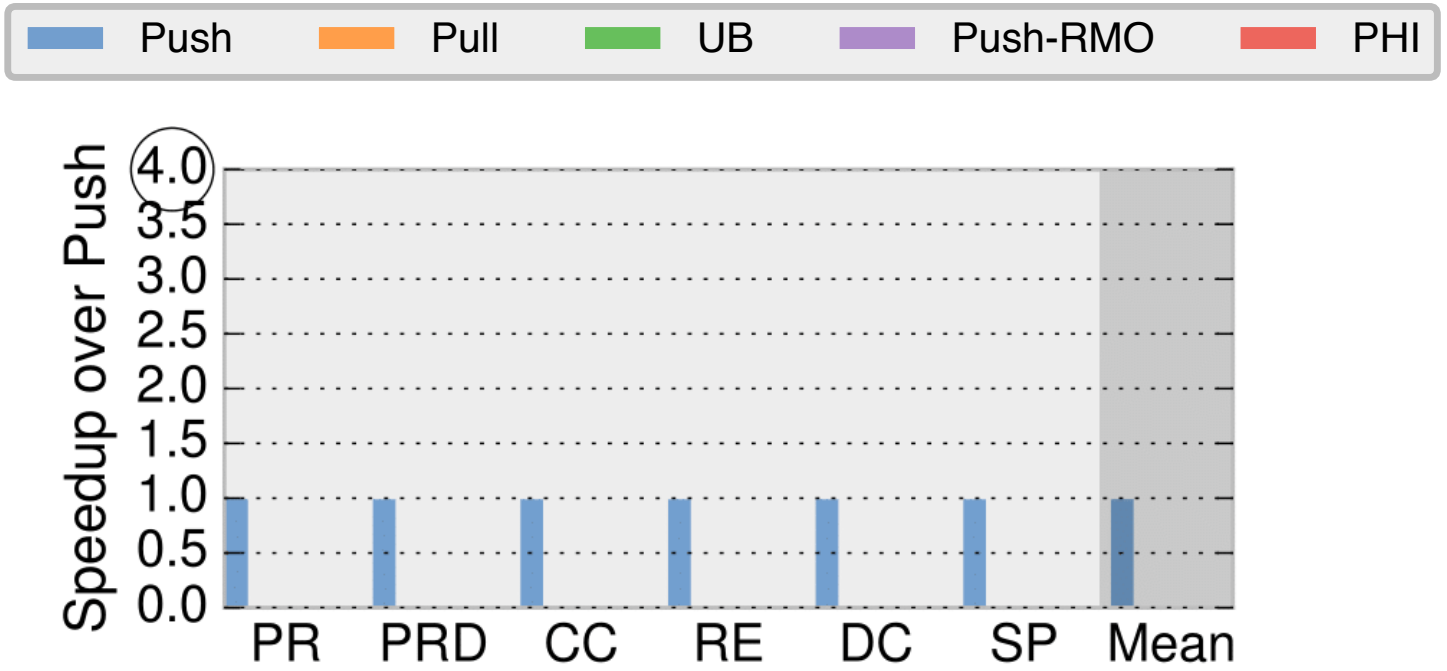

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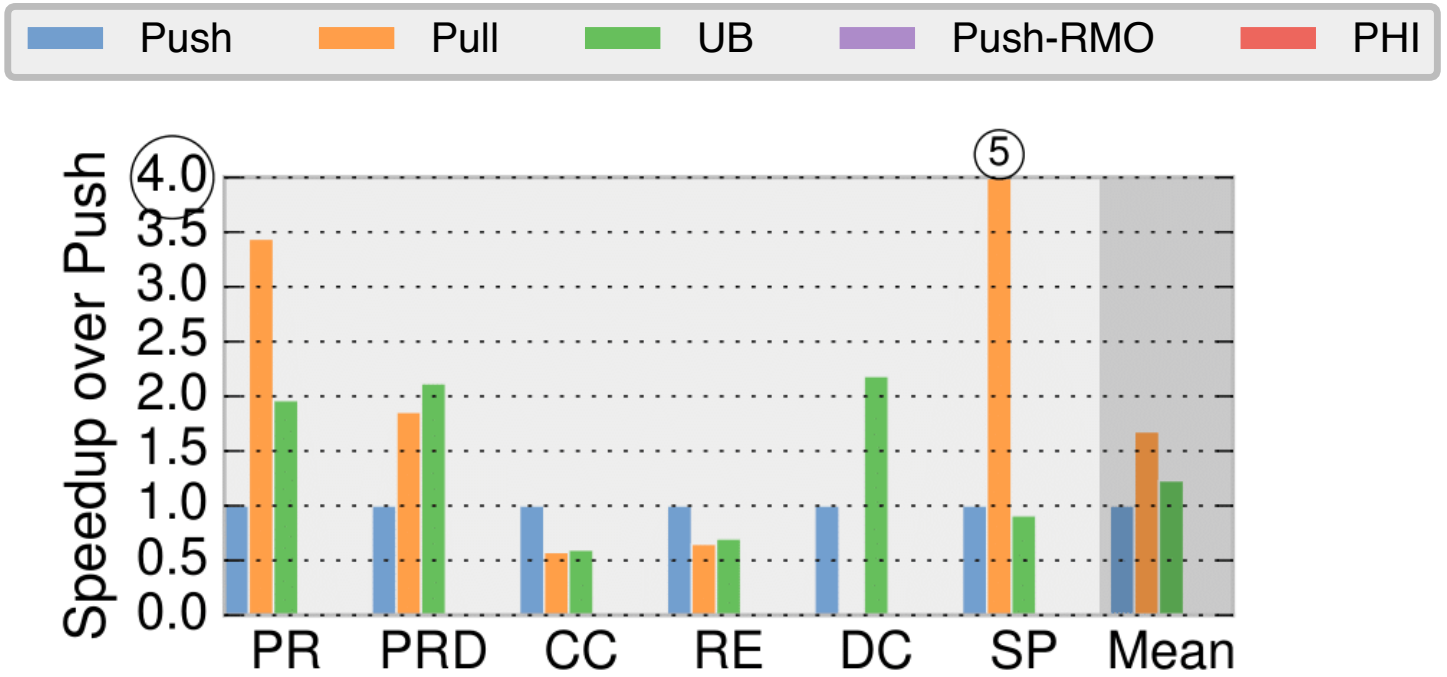

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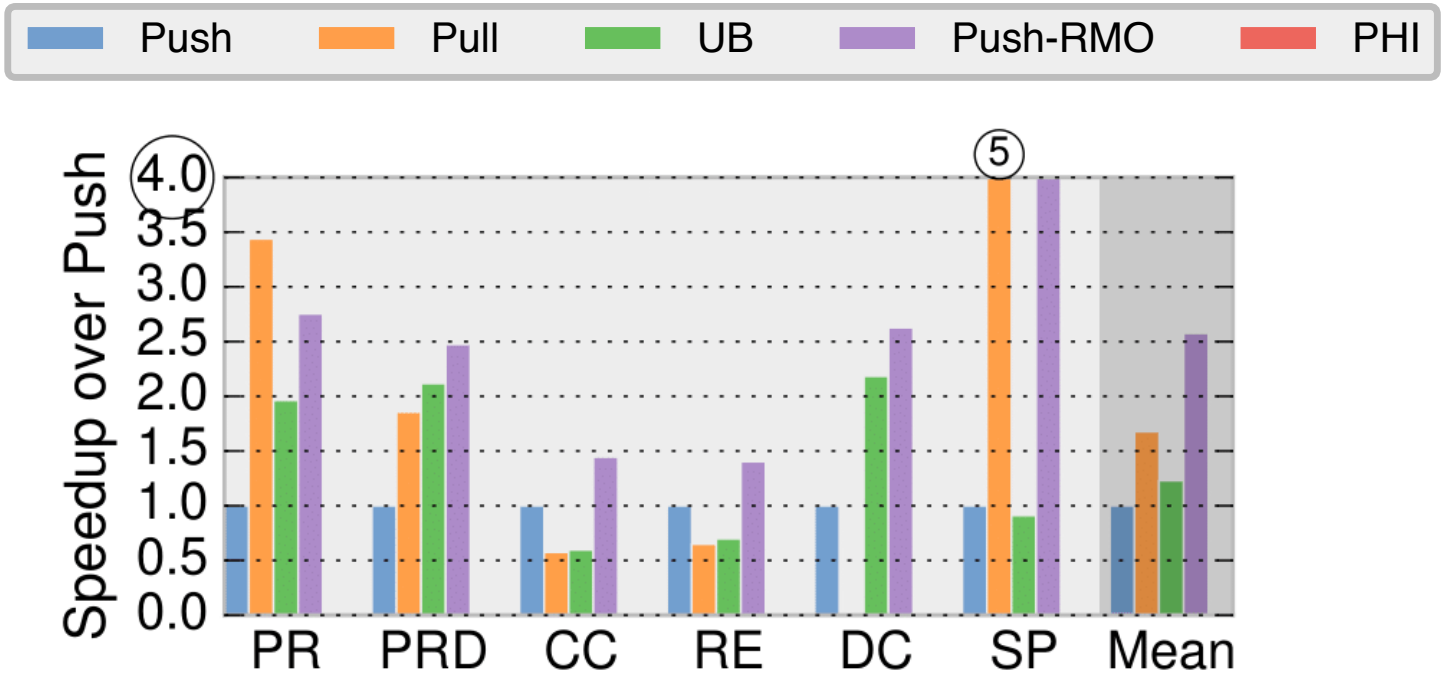

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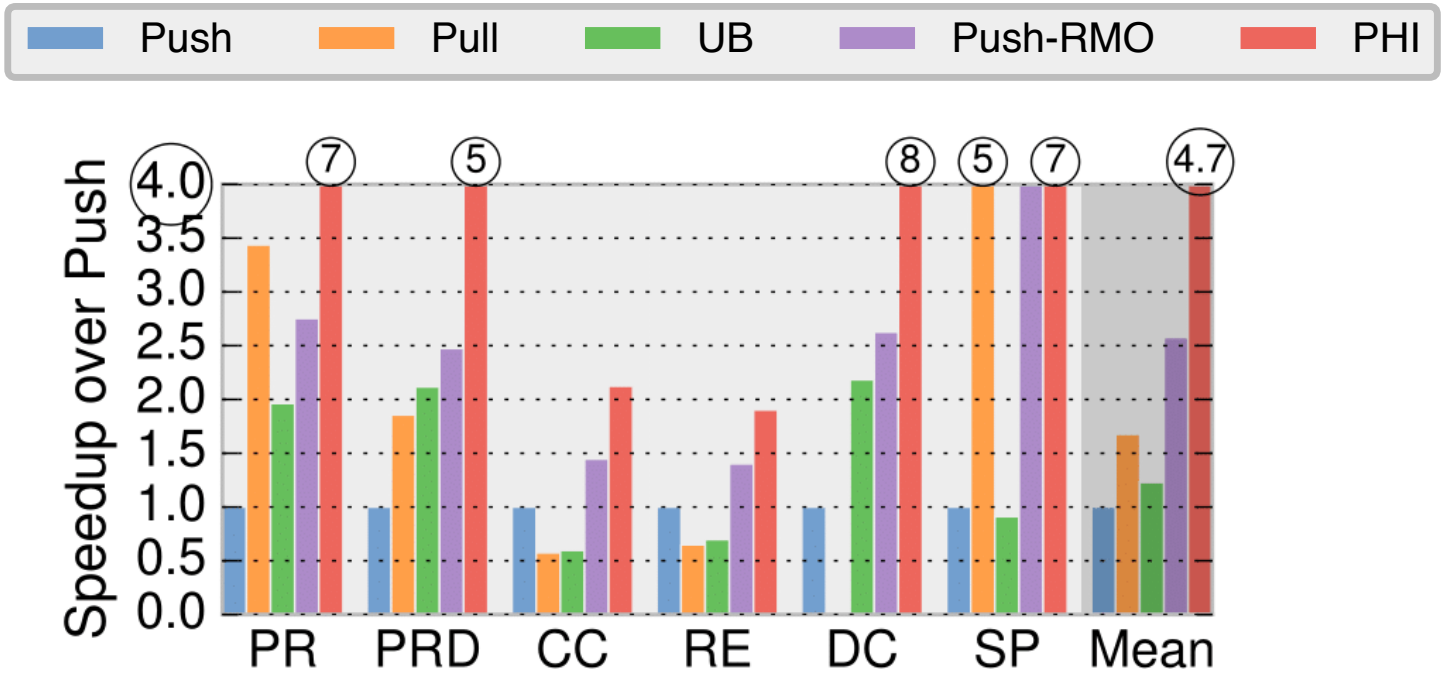

- Pull and UB show mixed results
- Push-RMO improves performance by avoiding synchronization costs
- PHI consistently outperforms other schemes

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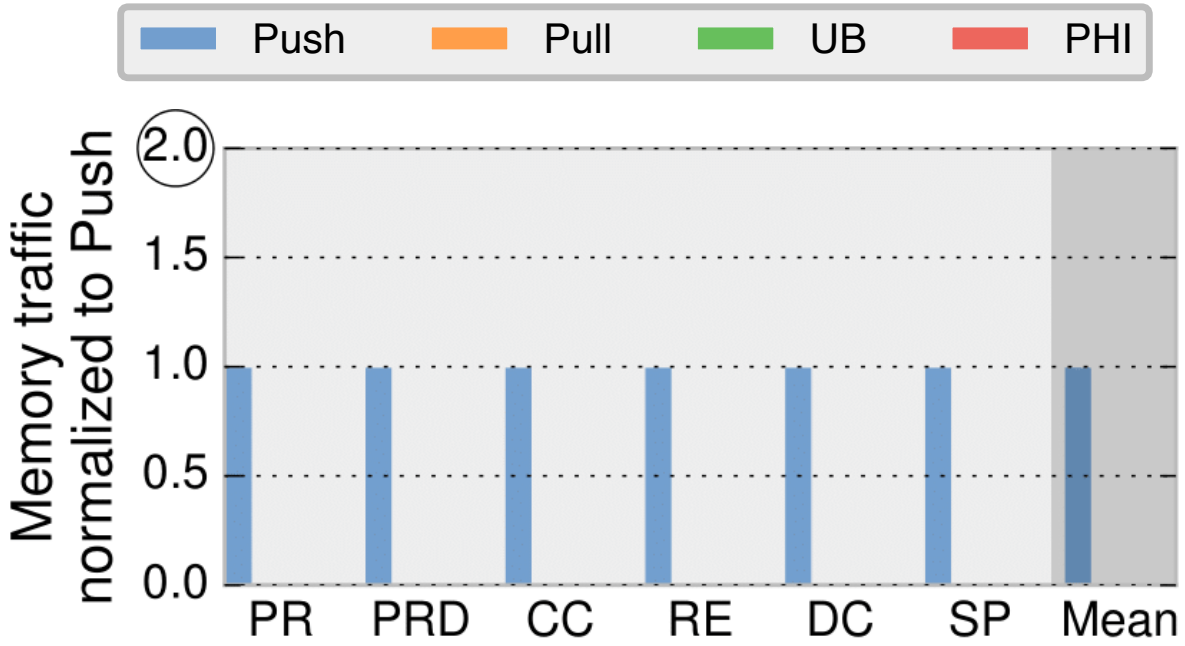

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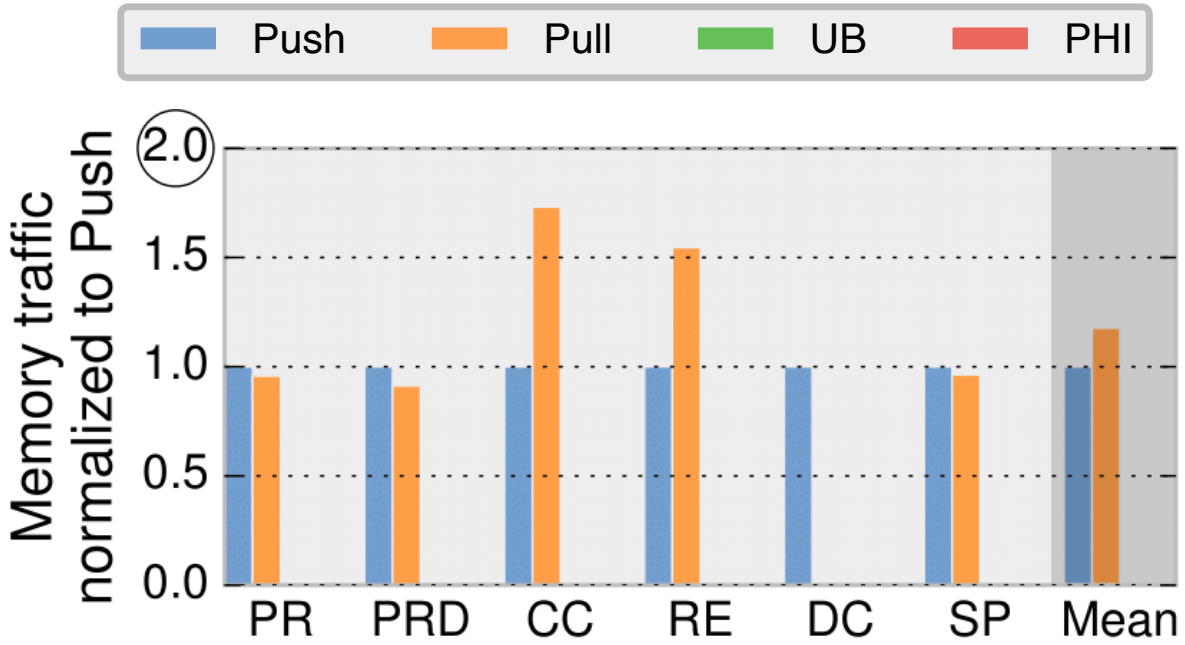

- Pull incurs higher memory traffic for non-all-active algorithms (CC, RE)

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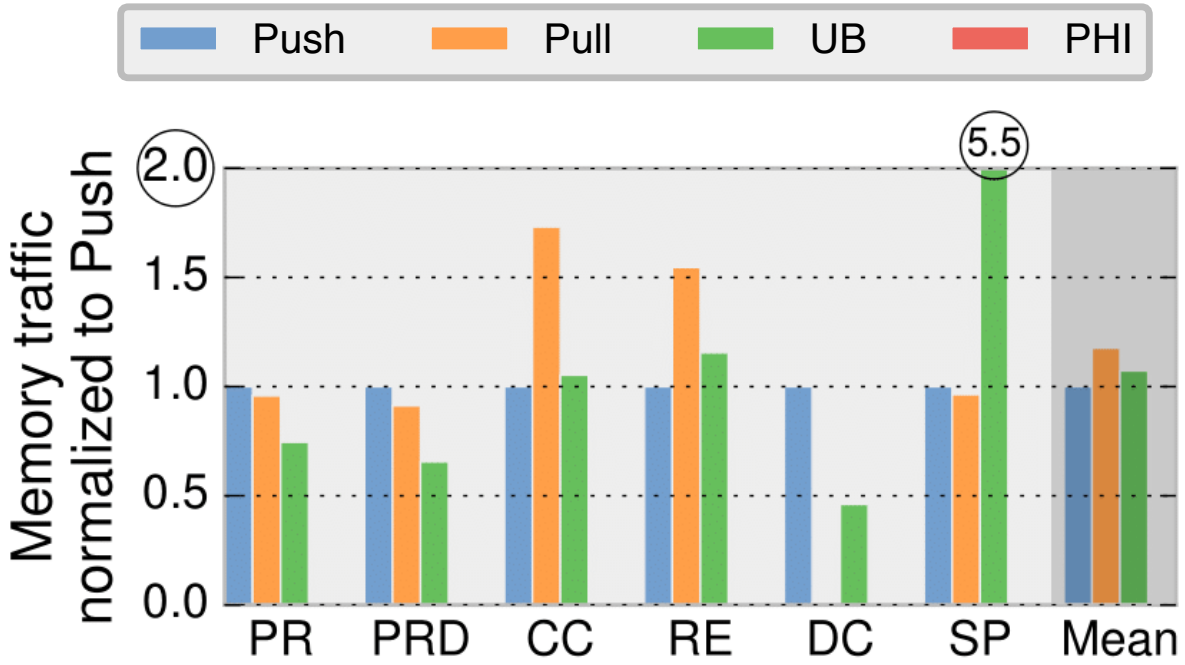

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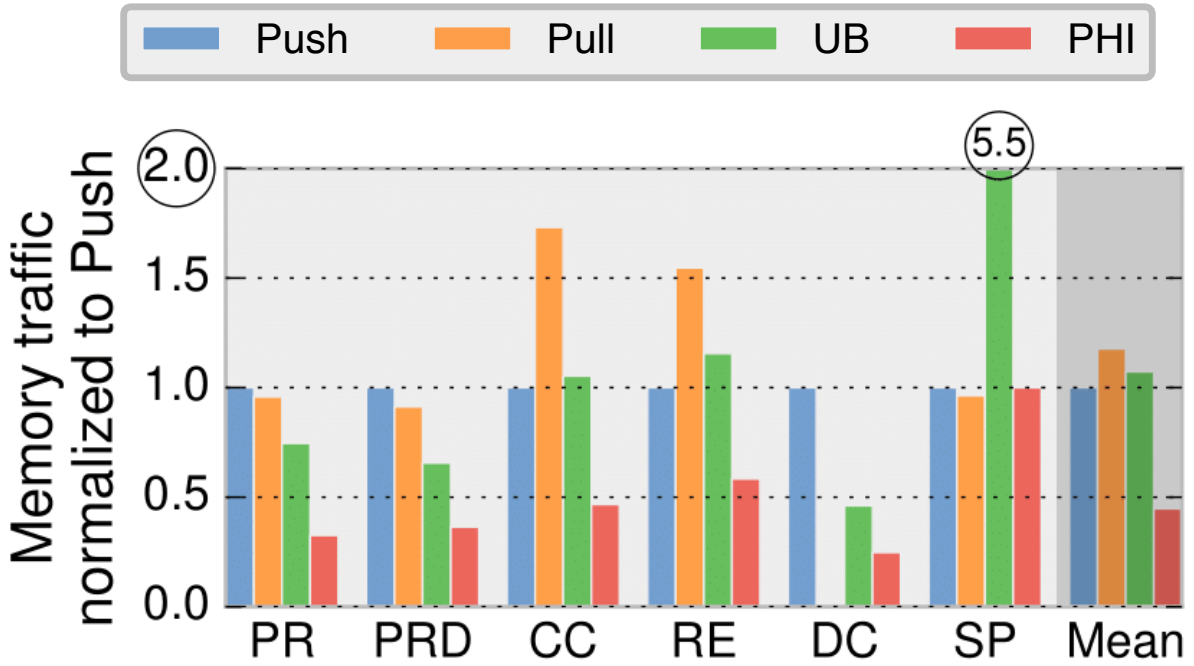

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- UB increases memory traffic when input has good locality
- PHI reduces memory traffic over UB by exploiting temporal locality

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Thanks For Your Attention!
Questions Are Welcome!